EPIC-QM77

Intel® Core™ i7/i5/i3/Celeron® Processor

Supports DDR3/L 1333/1600 Memory

18/24-bit Single/Dual Channel LVDS

CRT, DVI-I, HDMI

2 USB 3.0, 4 USB2.0, 6 COMs, 2 SATA

16-bit Digital I/O Co-lay with LPT

EPIC-QM77 Manual 1st Ed.
June. 2013

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Packing List

Before you begin installing your card, please make sure that the following materials have been shipped:

- Product DVD
- EPIC-QM77
- 1702150155 SATA Power Cable
- 1709070500 SATA Cable
- M10QM77000 Heat Spreader
- 9657666600 Jumper Cap

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

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Chapter 1

General Information

1.1 Introduction

AAEON announces a brand new EPIC Board EPIC-QM77, designed to fit in diverse applications that demand for fitting in different space limitations and high performance.

EPIC-QM77 accommodates onboard Intel® Core™ i7/i5/i3/Celeron® Processor and features one socket for a 204-pin DDR3/L 1333/1600 SODIMM for up to 8GB of system memory. Moreover, EPIC-QM77 adopts Intel® QM77 chipset to achieve an excellent performance.

In addition, EPIC-QM77 deploys two Intel® 82579LM and 82583V Ethernet chips to feature two RJ-45 ports onboard to display the transcendent performance of network connections. The display chipset of EPIC-QM77 is integrated to Intel® CPU and integrated Graphics support CRT/LCD simultaneous/ dual view displays.

In addition to the PCI-104 expansion, EPIC-QM77 also features two SATA3, two USB 3.0 ports, four USB 2.0 ports, six COM ports, one Mini Card slot, 16-bit Digital I/O Co-lay with LPT for flexible I/O expansion. EPIC-QM77 is an excellent choice for your vital applications.

1.2 Features

- Intel® Core™ i7/i5/i3/Celeron® Processor
- Intel® QM77/HM76
- SODIMM DDR3/L 1333/1600MHz Memory, Max. 8GB
- Gigabit Ethernet x 2
- Up To 24-bit Dual-channel LVDS LCD
- 2CH HD Audio
- SATA 6.0Gb/s x 2, mSATA (Full-Size) Slot x 1
- USB 3.0 x 2, USB2.0 x 4, COM x 6, 16-bit Digital I/O Co-lay with LPT
- PCI-104: 2 x Mini-PCIe socket (one for mSATA, one for Mini card)
- +12V DC Input

1.3 Specifications

System

Form Factor	EPIC Express Board
Processor	Intel® Core™ i7/i5/i3/Celeron® Processor
System Memory	204-pin SODIMM DDR3/L 1333/1600MHz Memory, Max. 8 GB
Chipset	Intel® QM77/HM76
I/O Chipset	Fintek 81866D
Ethernet	Intel 82579LM x 1/Intel 82583V x 1 10/100/1000Base LANs, RJ-45 X2 Intel 82583V co-lay with Intel 82574L Support IEEE1588
BIOS	AMI BIOS 64Mbit SPI ROM
Wake On LAN	Yes
Watchdog Timer	Generates a time-out system reset
H/W Status Monitoring	Supports power supply voltages, fan speed, and temperature monitoring
Expansion Interface	PCI-104 connector
Battery	Lithium battery
Power Requirement (Typical)	+12V

- Board Size: 4.5" x 6.5" (115mm x 165mm)
- Gross Weight: 0.88 lb (0.4 Kg)
- Operation Temperature: 32°F ~ 140°F (0°C ~ 60°C)
- Storage Temperature: -4°F ~158°F (-20°C ~70°C)
- Operation Humidity: 10~80%, non-condensing

Display: Supports CRT/LCD simultaneous/ dual view displays

- Chipset: Intel® 3rd Core™ i7/i5/i3/Celeron®
- Memory: Shared system memory up to 512 MB
- Resolutions: Up to 2048 x 1536 @ 75 Hz for CRT
  Up to 1920 x 1200 @85Hz for LCD (Pixel clock 25-112 Mhz)
  Up to 1920 x 1200p @ 60 Hz for DVI
  Up to 1920 x 1200p @60Hz for HDMI
- LCD Interface: 24-bit dual-channel LVDS

I/O

- Storage: SATA 2 x 2 (Support RAID 0,1), 2 Mini card sockets (1 x Mini card, 1 x mSATA)
- Serial Port: RS-232/422/485 x 1,

	supports 5/12V on D-Sub connector (COM 2) on rear I/O COM1 stack up on top of COM2; 4 COM ports on box head
● Parallel Port	SPP/EPP/ECP Mode
● USB	4 USB 2.0 with box header, 2 USB3.0 on rear I/O
● PS/2 Port	Keyboard x 1, Mouse x 1
● Digital I/O	Supports 16-bit (programmable)
● Audio	Line-in, Line-out, Mic-in & CD-in

Chapter 2

Quick Installation Guide

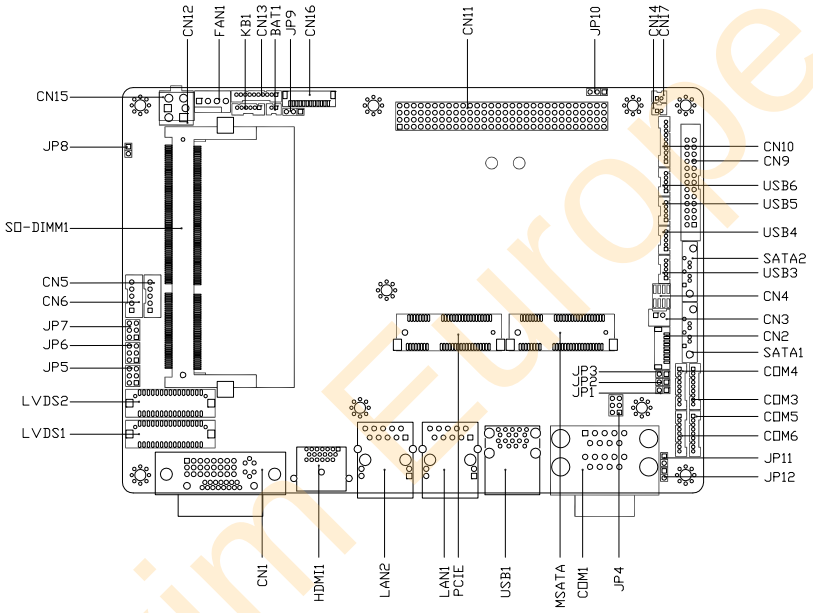
2.1 Safety Precautions

Always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on, because a sudden rush of power can damage sensitive electronic components.

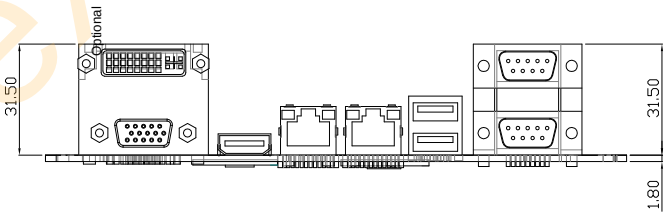
Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis

2.2 Location of Connectors and Jumpers

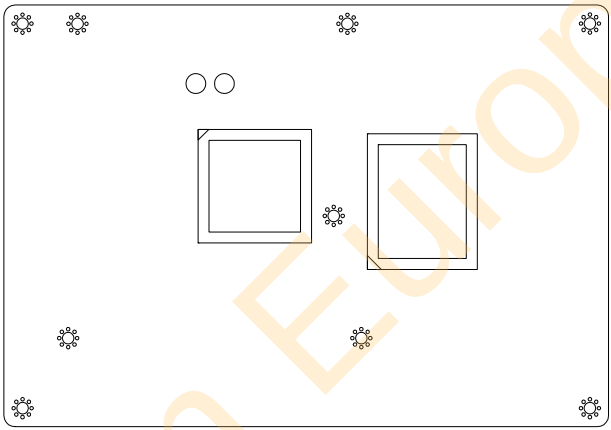
Component Side



Component Side



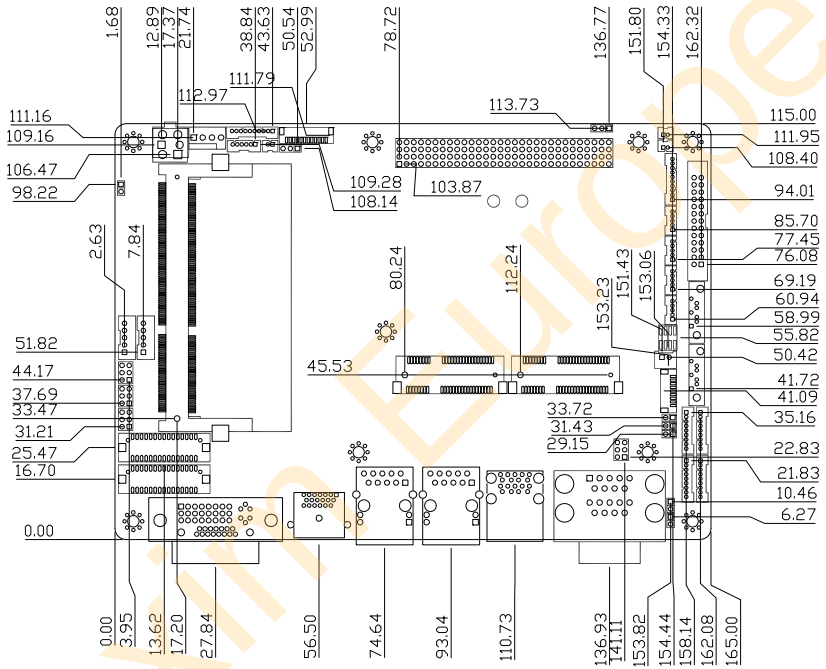
Solder Side



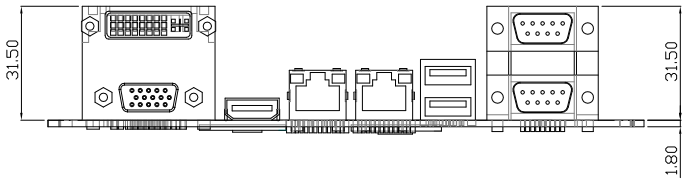
Solder Side

2.3 Mechanical Drawing

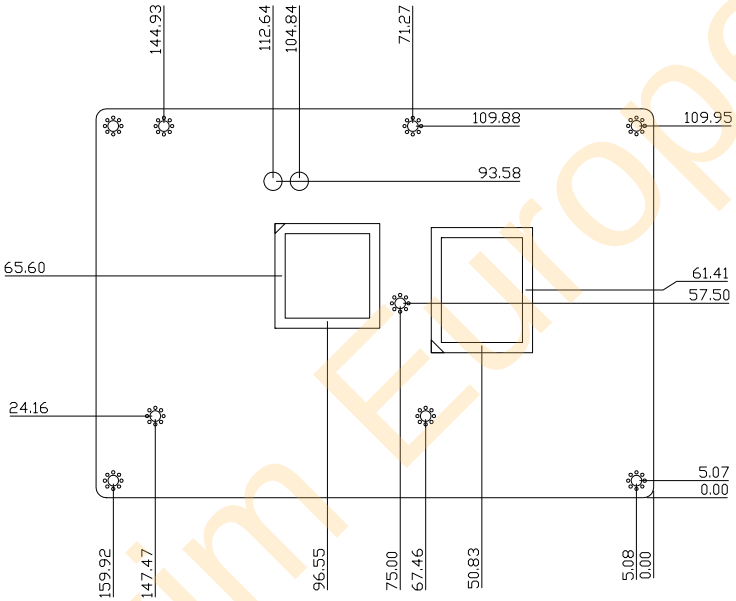
Component Side



Component Side



Solder Side



Solder Side

2.4 List of Jumpers

The board has a number of jumpers that allow you to configure your system to suit your application.

The table below shows the function of each of the board's jumpers:

Jumpers

Label	Function
JP1	LPT_DIO Selection
JP2	AT/ATX Selection
JP3	Touch Screen Connector Selection
JP4	Ring_12V_5V Selection
JP5	LCD VCC Selection
JP6	LCD Backlight Voltage Selection
JP7	LCD Backlight Control Selection
JP8	DDR3/DDR3L Voltage Selection
JP9	Clear CMOS
JP10	VIO104 Power Selection
JP11	mSATA _ PCI-e Selection
JP12	COM2 Slew Selection

2.5 List of Connectors

The board has a number of connectors that allow you to configure your system to suit your application. The table below shows the function of each board's connectors:

Connectors

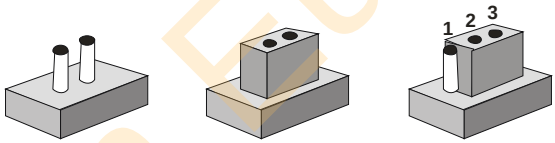
Label	Function
CN1	VGA / DVI Dual Connector
CN2	Touch Screen Connector
CN3	SATA Power Connector
CN4	SPI Flash Header
CN5	1st Backlight Connector
CN6	2nd Backlight Connector
CN7	1st Mini Card Slot
CN8	2nd Mini Card Slot
CN9	LPT_DIO Connector
CN10	Audio Connector
CN11	PCI-104 Slot
CN12	4-Pin Power In Connector
CN13	Front Panel Connector
CN14	Amp R-channel Connector
CN15	2-Pin Power in Connector
CN16	LPC Connector
CN17	Amp L-channel Connector
CN18	3G SIM Connector

LAN1	1000 Base-Tx Ethernet Connector
LAN2	1000 Base-Tx Ethernet Connector
USB1	Dual USB3.0 Connector
USB3	USB2.0 Connector
USB4	USB2.0 Connector
USB5	USB2.0 Connector
USB6	USB2.0 Connector
COM1(Dual A)	COM1 RS-232 Serial Port Connector
COM1(Dual B)	COM2 RS-232/422/485 Serial Port Connector
COM3	COM3 RS-232 Serial Port Connector
COM4	COM4 RS-232 Serial Port Connector
COM5	COM5 RS-232 Serial Port Connector
COM6	COM6 RS-232 Serial Port Connector
SATA1	SATA Connector
SATA2	SATA Connector
KB1	PS/2 Keyboard Mouse Connector
FAN1	Fan Connector
HDMI1	HDMI Connector
BAT1	RTC Battery Connector
LVDS1	1st LVDS Connector
LVDS2	2nd LVDS Connector

2.6 Setting Jumpers

You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.

To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.

2.7 LPD_DIO Selection (JP1)

LPT

DIO

JP1	Function
Off	LPT
On	DIO

2.8 AT/ATX Selection (JP2)

ATX

AT

JP2	Function
Off	ATX
On	AT

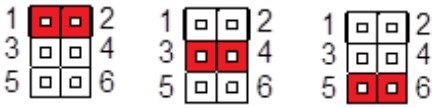
2.9 Touch Screen Selection (JP3)

4,8 Wire

5 Wire

JP3	Function
Off	5 Wire
On	4.8 Wire

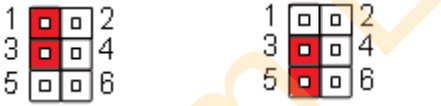
2.10 Ring_12V_5V Selection (JP4)



+12V RI2# +5V

JP4	Function
1-2	+12V
3-4	RI2#_SEL
5-6	+5V

2.11 LCD VCC Selection (JP5)



LVDS1 +5V LVDS1 +3.3V

LVDS 1

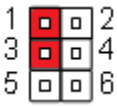
LVDS 1	Function
1-3	+5V (Default)
3-5	+3.3V

LVDS2 +5V LVDS2 +3.3V

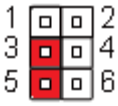
LVDS 2

LVDS 2	Function
2-4	+5V (Default)
4-6	+3.3V

2.12 LCD Backlight Voltage Selection (JP6)



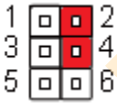
LVDS1 +5V



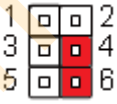
LVDS1 +12V

LVDS 1

LVDS 1	Function
1-3	+5V (Default)
3-5	+12V



LVDS2 +5V

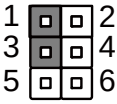


LVDS2 +12V

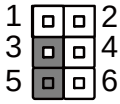
LVDS 2

LVDS 2	Function
2-4	+5V (Default)
4-6	+12V

2.13 LCD Backlight Control Selection (JP7)



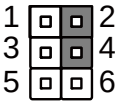
LVDS1 Voltage-mode



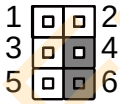
LVDS1 PWM-mode

LVDS 1

LVDS 1	Function
1-3	Voltage-mode
3-5	PWM-mode



LVDS2 Voltage-mode



LVDS2 PWM-mode

LVDS 2

LVDS 2	Function
2-4	Voltage-mode
4-6	PWM-mode

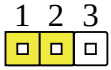
2.14 DDR _DDRL Selection (JP8)

DDR3

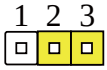
DDR3L

JP8	Function
Off	DDR3
On	DDR3L

2.15 Clear CMOS Selection (JP9)



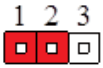
NORMAL



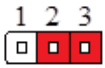
CLEAR CMOS

JP9	Function
1-2	NORMAL
2-3	CLEAR CMOS

2.16 PCI-104 I/O Voltage Selection (JP10)



+5V



+3.3V

JP10	Function
1-2	+5V
2-3	+3.3V

2.17 mSATA_PCIe Selection (JP11)

mSATA

PCIe

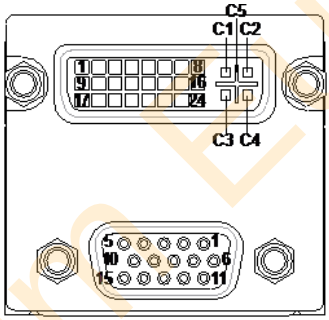
JP11	Function
Off	mSATA
On	PCIe

2.18 COM2 Slew Selection (JP12)

250k 1M/10M

JP12	Function
Off	250k
On	1M/10M

2.19 VGA & DVI-I CONNECTOR (CN1)



VGA

Pin	Pin Name	Signal Type	Signal Level
1	RED	I/O	
3	BLUE	I/O	
5	GND	GND	
7	GND	GND	
9	V5S_DISP	PWR	5V
11	NC		
13	HSYNC	I/O	
15	DDC_CLK	I/O	

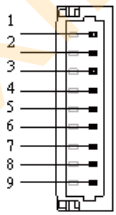
Pin	Pin Name	Signal Type	Signal Level
2	GREEN	I/O	
4	NC		
6	GND	GND	
8	GND	GND	
10	CRT_PLUG#	IN	
12	DDC_DATA	I/O	
14	VSYNC	I/O	

DVI

Pin	Pin Name	Signal Type	Signal Level
1	DVI_DATA2_N	I/O	
3	GND	GND	
5	NC		
7	DVI_SDA	I/O	
9	DVI_DATA1_N	I/O	
11	GND	GND	
13	NC		
15	D_CRT_PLUG#	IN	
17	DVI_DATA0_N	I/O	
19	GND	GND	
21	NC		
23	DVI_CLK_P	I/O	
C1	RED	I/O	
C3	BLUE	I/O	
C5	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
2	DVI_DATA2_P	I/O	
4	NC		
6	DVI_SCL	I/O	
8	VSYNC	I/O	
10	DVI_DATA1_P	I/O	
12	NC		
14	V5S_DISP	PWR	5V
16	DVI_HPD	I/O	
18	DVI_DATA0_P	I/O	
20	NC		
22	GND	GND	
24	DVI_CLK_N	I/O	
C2	GREEN	I/O	
C4	HSYNC	I/O	
C6	GND	GND	

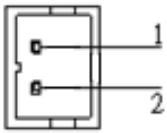
2.20 Touch Screen Connector (CN2)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	Y-	IN	
3	Y+	IN	

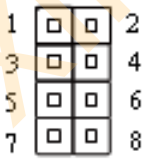
4	X-	IN
5	X+	IN
6	SENSE	IN
7	Y+	IN
8	X-	IN
9	X+	IN

2.21 SATA Power Connector (CN3)



Pin	Pin Name	Signal Type	Signal Level
1	V5S	PWR	+5V
2	GND	GND	GND

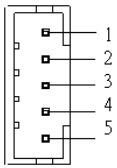
2.22 SPI Flash Header (CN4)



Pin	Pin Name	Signal Type	Signal Level
1	V3.3M_SPI	PWR	+3.3V
3	SPI_CE#_F	IN	
5	SPI_SO_F	OUT	
7			

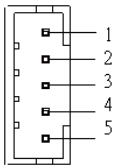
Pin	Pin Name	Signal Type	Signal Level
2	GND	GND	
4	SPI_CLK_F	I/O	
6	SPI_SI_F	IN	
8			

2.23 1st Backlight Connector (CN5)



Pin	Pin Name	Signal Type	Signal Level
1	VCC_LVDS_BKLT1	PWR	+5V OR +12V
2	L_BRIGHTNESS1	OUT	
3	GND	GND	
4	GND	GND	
5	BKLT_EN1	OUT	

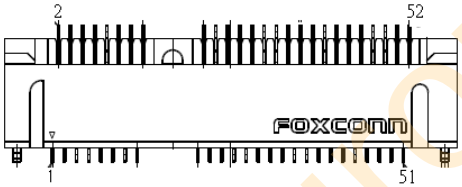
2.24 2nd Backlight Connector (CN6)



Pin	Pin Name	Signal Type	Signal Level
1	VCC_LVDS_BKLT2	PWR	+5V OR +12V
2	L_BRIGHTNESS2	OUT	

3	GND	GND
4	GND	GND
5	BKLT_EN2	OUT

2.25 m-SATA Mini-Card Connector (CN7)



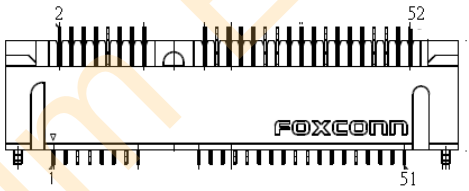
Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	OUT	
3	Reserved		
5	Reserved		
7	CLK_PCIE_REQ#_M PCIE	OUT	
9	GND	GND	
11	CLK_PCIE_MPCIE_ N	I/O	
13	CLK_PCIE_MPCIE_ P	I/O	
15	GND	GND	
17	Reserved		
19	Reserved		
21	XSD	OUT	
23	PERn0_RX+	I/O	
25	PERp0_RX-	DIFF	
27	GND	GND	
29	GND	GND	
31	PETn0_TX-	I/O	

33	PETp0_TX+	I/O	
35	GND	GND	
37	GND	GND	
39	+V3.3_MINICARD1	PWR	+3.3V
41	+V3.3_MINICARD1	PWR	+3.3V
43	NC		
45	Reserved	I/O	
47	Reserved	I/O	
49	Reserved	I/O	
51	Reserved	I/O	

Pin	Pin Name	Signal Type	Signal Level
2	V3.3_MINICARD1	PWR	+3.3V
4	GND	GND	
6	+V1.5S	PWR	+1.5V
8	Reserved		
10	Reserved		
12	Reserved		
14	Reserved		
16	Reserved		
18	Reserved		
20	MINI_DISABLE#	IN	
22	BUF_PLT_RST#	IN	
24	+V3.3_MINICARD1	PWR	+3.3V
26	GND	GND	
28	+V1.5S	PWR	+1.5V
30	SMB_CLK_SBY	I/O	

32	SMB_DATA_SBY	I/O	
34	GND	GND	
36	USB_PN2	I/O	
38	USB_PP2	I/O	
40	GND	GND	
42	Reserved		
44	Reserved		
46	Reserved		
48	+V1.5S	PWR	+1.5V
50	GND	GND	
52	+V3.3_MINICARD1	PWR	+3.3V

2.26 PCI-E Mini-Card Connector (CN8)



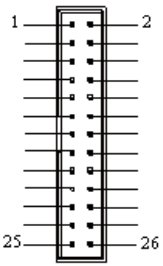
Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	OUT	
3	Reserved		
5	Reserved		
7	CLK_PCIE_REQ#_MINI2	OUT	
9	GND	GND	
11	CLK_PCIE_MINI2_N	I/O	
13	CLK_PCIE_MINI2_P	I/O	
15	GND	GND	

17	Reserved		
19	Reserved		
21	GND	GND	
23	PCIE_RXN6	I/O	
25	PCIE_RXP6	I/O	
27	GND	GND	
29	GND	GND	
31	PCIE_TNX6	I/O	
33	PCIE_TXP6	I/O	
35	GND	GND	
37	GND	GND	
39	+V3.3_MINICARD2	PWR	+3.3V
41	+V3.3_MINICARD2	PWR	+3.3V
43	Reserved		
45	Reserved		
47	CL_CLK	I/O	
49	CL_DATA	I/O	
51	CL_RST#	IN	

Pin	Pin Name	Signal Type	Signal Level
2	+V3.3_MINICARD2	PWR	+3.3V
4	GND	GND	
6	+V1.5S	PWR	+1.5V
8	Reserved		
10	Reserved		
12	Reserved		
14	Reserved		

16	Reserved		
18	Reserved		
20	MINI_DISABLE#	IN	
22	BUF_PLT_RST#	IN	
24	+V3.3_MINICARD2	PWR	+3.3V
26	GND	GND	
28	+V1.5S	PWR	+1.5V
30	SMB_CLK_SBY	I/O	
32	SMB_DATA_SBY	I/O	
34	GND	GND	
36	USB_PN7	I/O	
38	USB_PP7	I/O	
40	GND	GND	
42	Reserved		
44	Reserved		
46	Reserved		
48	+V1.5S	PWR	+1.5V
50	GND	GND	
52	+V3.3_MINICARD2	PWR	+3.3V

2.27 LPT Port Connector (CN9)



LPT Mode:

Pin	Pin Name	Signal Type	Signal Level
1	STOBE#	I/O	
3	PPD0	I/O	
5	PPD1	I/O	
7	PPD2	I/O	
9	PPD3	I/O	
11	PPD4	I/O	
13	PPD5	I/O	
15	PPD6	I/O	
17	PPD7	I/O	
19	ACK#	I/O	
21	BUSY	I/O	
23	PE	I/O	
25	SLCT	I/O	

Pin	Pin Name	Signal Type	Signal Level
2	#AFD	I/O	
4	ERR#	I/O	
6	PINIT#	I/O	
8	SLIN#	I/O	
10	GND	GND	
12	GND	GND	
14	GND	GND	
16	GND	GND	
18	GND	GND	

20	GND	GND
22	GND	GND
24	GND	GND
26	N.C	

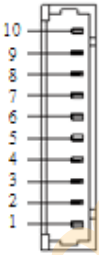
DIO Mode:

Pin	Pin Name	Signal Type	Signal Level
1	GPIO7	I/O	
3	GPIO8	I/O	
5	GPIO9	I/O	
7	GPIO10	I/O	
9	GPIO11	I/O	
11	GPIO12	I/O	
13	GPIO13	I/O	
15	GPIO14	I/O	
17	GPIO15	I/O	
19	GPIO2	I/O	
21	GPIO1	I/O	
23	GPIO0	I/O	
25	N.C		

Pin	Pin Name	Signal Type	Signal Level
2	GPIO6	I/O	
4	GPIO5	I/O	
6	GPIO4	I/O	
8	GPIO3	I/O	
10	GND	GND	

12	GND	GND
14	GND	GND
16	GND	GND
18	GND	GND
20	GND	GND
22	GND	GND
24	GND	GND
26	N.C	

2.28 Audio Connector (CN10)

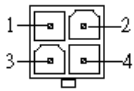


Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_R	IN	
3	GND_AUDIO	GND	
4	LIN_L	IN	
5	LIN_R	IN	
6	GND_AUDIO	GND	
7	LOUT_L	OUT	
8	GND_AUDIO	GND	
9	LOUT_R	OUT	
10	+5V_AUDIO	PWR	+5V

2.29 PCI-104 Connector (CN11)

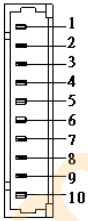
	A	B	C	D
1	GND	+5V_SB	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	PSON#	PAR
10	GND	PERR#	+3.3V	PME#
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

2.30 ATX 4Pin Power Connector (CN12)



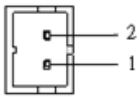
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
3	+12VSB	PWR	+12V
2	GND	GND	
4	+12VSB	PWR	+12V

2.31 Front Panel Connector(CN13)



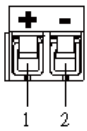
Pin	Pin Name	Signal Type	Signal Level
1	PWRSIN#	IN	
2	GND	GND	
3	+V5S	PWR	+5V
4	FP_SPKR#	IN	
5	+V3.3S	PWR	+3.3V
6	FP_HDLED#	IN	
7	+V3.3S	PWR	+3.3V
8	GND	GND	
9	HWRST#	IN	
10	GND	GND	

2.32 AMP-R Channel Connector (CN14)



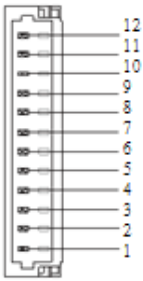
Pin	Pin Name	Signal Type	Signal Level
1	SPK_R+	OUT	
2	SPK_R-	OUT	

2.33 2Pin Power Connector (CN15)



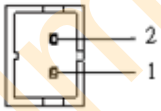
Pin	Pin Name	Signal Type	Signal Level
1	+12VSB	PWR	+12V
2	GND	GND	

2.34 LPC Connector (CN16)



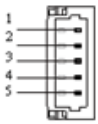
Pin	Pin Name	Signal Type	Signal Level
1	LPC_AD0	I/O	
2	LPC_AD1	I/O	
3	LPC_AD2	I/O	
4	LPC_AD3	I/O	
5	+V3.3S	PWR	+3.3V
6	LPC_FRAME#	IN	
7	BUF_PLT_RST#	IN	
8	GND	GND	
9	CLK_LPC_33M	OUT	
10	LPC_DRQ#0	OUT	
11	LPC_DRQ#1	OUT	
12	INT_SERIRQ	I/O	

2.35 AMP-L Channel Connector (CN17)



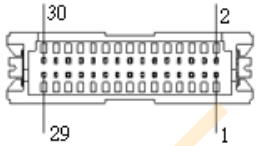
Pin	Pin Name	Signal Type	Signal Level
1	SPK_L+	OUT	
2	SPK_L-	OUT	

2.36 3G SIM Connector (CN18)



Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	+3.3V
2	UIM_DAT	I/O	
3	UIM_CLK	OUT	
4	UIM_RST	OUT	
5	UIM_VPP	GND	

2.37 1st LVDS Connector (LVDS1)

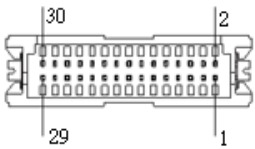


Pin	Pin Name	Signal Type	Signal Level
1	BKLT_EN1	OUT	
3	+VDD_LVDS1	PWR	+3.3V OR +5V
5	LVDSA_CLK#	OUT	
7	+VDD_LVDS1	PWR	+3.3V OR +5V
9	LVDSA_DATA0#	I/O	
11	LVDSA_DATA1#	I/O	
13	LVDSA_DATA2#	I/O	
15	LVDSA_DATA3#	I/O	
17	LVDS_DDC_DATA	I/O	
19	LVDSB_DATA0#	I/O	
21	LVDSB_DATA1#	I/O	
23	LVDSB_DATA2#	I/O	
25	LVDSB_DATA3#	I/O	
27	+VDD_LVDS1	PWR	+3.3V OR +5V

29	LVDSB_CLK#	I/O	

Pin	Pin Name	Signal Type	Signal Level
2	L_BRIGHTNESS1	OUT	
4	GND	GND	
6	LVDSA_CLK	OUT	
8	GND	GND	
10	LVDSA_DATA0	I/O	
12	LVDSA_DATA1	I/O	
14	LVDSA_DATA2	I/O	
16	LVDSA_DATA3	I/O	
18	LVDS_DDC_CLK	I/O	
20	LVDSB_DATA0	I/O	
22	LVDSB_DATA1	I/O	
24	LVDS_DATA2	I/O	
26	LVDSB_DATA3	I/O	
28	GND	GND	
30	LVDSB_CLK	I/O	

2.38 2nd LVDS Connector (LVDS2)



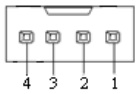
Pin	Pin Name	Signal Type	Signal Level
1	BKLT_EN2	OUT	

3	+VDD_LVDS2	PWR	+3.3V OR +5V
5	LVDSC_CLK#	I/O	
7	+VDD_LVDS2	PWR	+3.3V OR +5V
9	LVDSC_DATA0#	I/O	
11	LVDSC_DATA1#	I/O	
13	LVDSC_DATA2#	I/O	
15	LVDSC_DATA3#	I/O	
17	LVDS_DDC_DATA_3460	I/O	
19	LVDSD_DATA0#	I/O	
21	LVDSD_DATA1#	I/O	
23	LVDSD_DATA2#	I/O	
25	LVDSD_DATA3#	I/O	
27	+VDD_LVDS2	PWR	+3.3V OR +5V
29	LVDSD_CLK#	I/O	

Pin	Pin Name	Signal Type	Signal Level
2	L_BRIGHTNESS2	OUT	
4	GND	GND	
6	LVDSC_CLK	I/O	
8	GND	GND	
10	LVDSC_DATA0	I/O	
12	LVDSC_DATA1	I/O	
14	LVDSC_DATA2	I/O	
16	LVDSC_DATA3	I/O	
18	LVDS_DDC_CLK_3460	I/O	
20	LVDSD_DATA0	I/O	
22	LVDSD_DATA1	I/O	

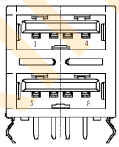
24	LVDSD_DATA2	I/O
26	LVDSD_DATA3	I/O
28	GND	GND
30	LVDSD_CLK	I/O

2.39 Fan Connector (FAN1)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	FAN_CTL	OUT	
3	FAN_TAC	OUT	
4	FAN_CTL_R	OUT	

2.40 USB3.0 Dual Connector (USB1)

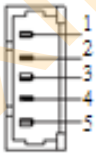


Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_0	PWR	+5V
3	USBD0+	I/O	
5	USB3_RX0_CON_N	I/O	
7	GND	GND	
9	USB3_TX0_CON_P	I/O	

11	USBD1-	I/O	
13	GND	GND	
15	USB3_RX1_CON_P	I/O	
17	USB3_TX1_CON_N	I/O	

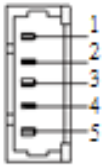
Pin	Pin Name	Signal Type	Signal Level
2	USBD0-	I/O	
4	GND	GND	
6	USB3_RX0_COP_P	I/O	
8	USB3_TX0_CON_N	I/O	
10	+V5A_USB_0	PWR	+5V
12	USBD1+	I/O	
14	USB3_RX1_CON_N	I/O	
16	GND	GND	
18	USB3_TX1_CON_P	I/O	

2.41 USB2.0 Connector (USB3)



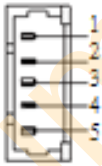
Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_2	PWR	+5V
2	USBD9-	I/O	
3	USBD9+	I/O	
4	GND	GND	
5	GND	GND	

2.42 USB2.0 Connector (USB4)



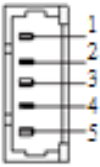
Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_2	PWR	+5V
2	USBD12-	I/O	
3	USBD12+	I/O	
4	GND	GND	
5	GND	GND	

2.43 USB2.0 Connector (USB5)



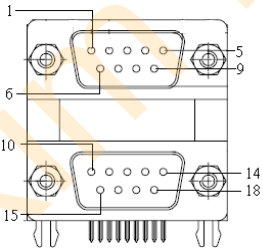
Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_3	PWR	+5V
2	USBD10-	I/O	
3	USBD10+	I/O	
4	GND	GND	
5	GND	GND	

2.44 USB2.0 Connector (USB6)



Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_3	PWR	+5V
2	USBD13-	I/O	
3	USBD13+	I/O	
4	GND	GND	
5	GND	GND	

2.45 RS-232 Serial Port Dual Connector (COM1)

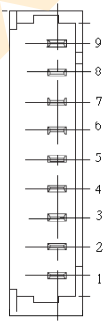


Pin	Pin Name	Signal Type	Signal Level
1	DCD#1	IN	
3	TXD1	OUT	
5	GND	GND	
7	RTS#1	OUT	
9	RI#1	IN	

11	RXD2(422RXD+)	IN
13	DTR#2(422RXD-)	OUT
15	DSR#2	IN
17	CTS#2	IN

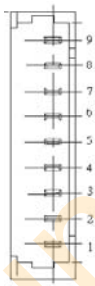
Pin	Pin Name	Signal Type	Signal Level
2	RXD#1	IN	
4	DTR#1	OUT	
6	DSR#1	IN	
8	CTS#1	IN	
10	DCD#2 (485D-)(422TXD-)	IN	
12	TXD2 (485D+)(422TXD+)	OUT	
14	GND	OUT	
16	RTS#2	OUT	
18	RI#2	IN	

2.46 RS-232 Serial Port Connector (COM3)



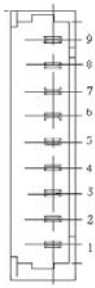
Pin	Pin Name	Signal Type	Signal Level
1	DCD#3	IN	
2	DSR#3	IN	
3	RXD3	IN	
4	RTS#3	OUT	
5	TXD3	OUT	
6	CTS#3	IN	
7	DTR#3	OUT	
8	RI#3	IN	

2.47 RS-232 Serial Port Connector (COM4)



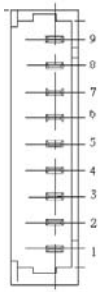
Pin	Pin Name	Signal Type	Signal Level
1	DCD#4	IN	
2	DSR#4	IN	
3	RXD4	IN	
4	RTS#4	OUT	
5	TXD4	OUT	
6	CTS#4	IN	
7	DTR#4	OUT	
8	RI#4	IN	
9	GND	GND	

2.48 RS-232 Serial Port Connector (COM5)



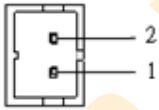
Pin	Pin Name	Signal Type	Signal Level
1	DCD#5	IN	
2	DSR#5	IN	
3	RXD5	IN	
4	RTS#5	OUT	
5	TXD5	OUT	
6	CTS#5	IN	
7	DTR#5	OUT	
8	RI#5	IN	
9	GND	GND	

2.49 RS-232 Serial Port Connector (COM6)



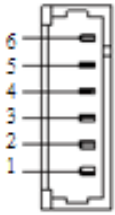
Pin	Pin Name	Signal Type	Signal Level
1	DCD#6	IN	
2	DSR#6	IN	
3	RXD6	IN	
4	RTS#6	OUT	
5	TXD6	OUT	
6	CTS#6	IN	
7	DTR#6	OUT	
8	RI#6	IN	
9	GND	GND	

2.50 Battery Connector (BAT1)



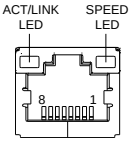
Pin	Pin Name	Signal Type	Signal Level
1	RTCBAT	PWR	+3.3V
2	GND	GND	

2.51 PS2 Keyboard and Mouse Connector (KB1)



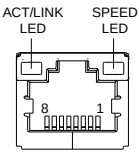
Pin	Pin Name	Signal Type	Signal Level
1	KBDATA	OUT	
2	KBCLK	OUT	
3	GND	GND	
4	+V5A_KBMS	PWR	+5V
5	MSDATA	OUT	
6	MSCLK	OUT	

2.52 LAN Ethernet RJ-45 Connector (LAN1)



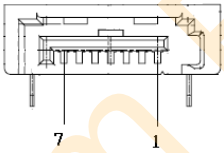
Pin	Pin Name	Signal Type	Signal Level
1	LAN1_MDIP0	I/O	
2	LAN1_MDIN0	I/O	
3	LAN1_MDIP1	I/O	
4	LAN1_MDIN1	I/O	
5	LAN1_MDIP2	I/O	
6	LAN1_MDIN2	I/O	
7	LAN1_MDIP3	I/O	
8	LAN1_MDIN3	I/O	

2.53 LAN Ethernet RJ-45 Connector (LAN2)



Pin	Pin Name	Signal Type	Signal Level
1	LAN2_MDIP0	I/O	
2	LAN2_MDIN0	I/O	
3	LAN2_MDIP1	I/O	
4	LAN2_MDIN1	I/O	
5	LAN2_MDIP2	I/O	
6	LAN2_MDIN2	I/O	
7	LAN2_MDIP3	I/O	
8	LAN2_MDIN3	DIFF.	
8	LAN1_MDIN3	I/O	

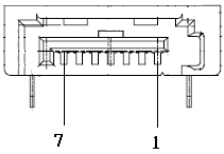
2.54 SATA CONNCETOR (SATA1)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
3	SATA_TXN0	I/O	
5	SATA_RXN0	I/O	
7	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
2	SATA_TXP0	I/O	
4	GND	GND	
6	SATA_RXP0	I/O	

2.55 SATA CONNCETOR (SATA2)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
3	SATA_TXN1	I/O	
5	SATA_RXN1	I/O	
7	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
2	SATA_TXP1	I/O	
4	GND	GND	
6	SATA_RXP1	I/O	

Below Table for China RoHS Requirements
产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	O	O	O	O	O
外部信号连接器及线材	×	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

Chapter 3

AMI BIOS Setup

3.1 System Test and Iinitialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The EPIC-QM77 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del>or <F2> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Boot

Enables/disable quiet boot option.

Security

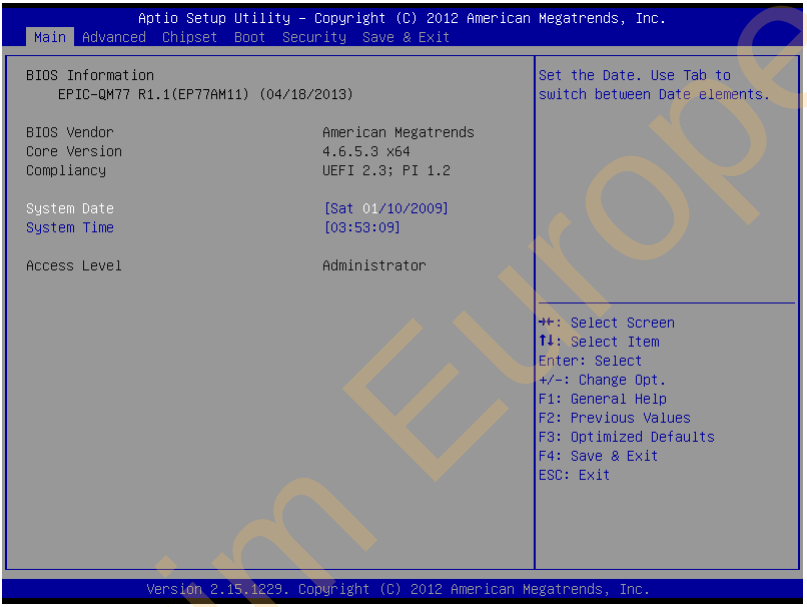
Set setup administrator password.

Save & Exit

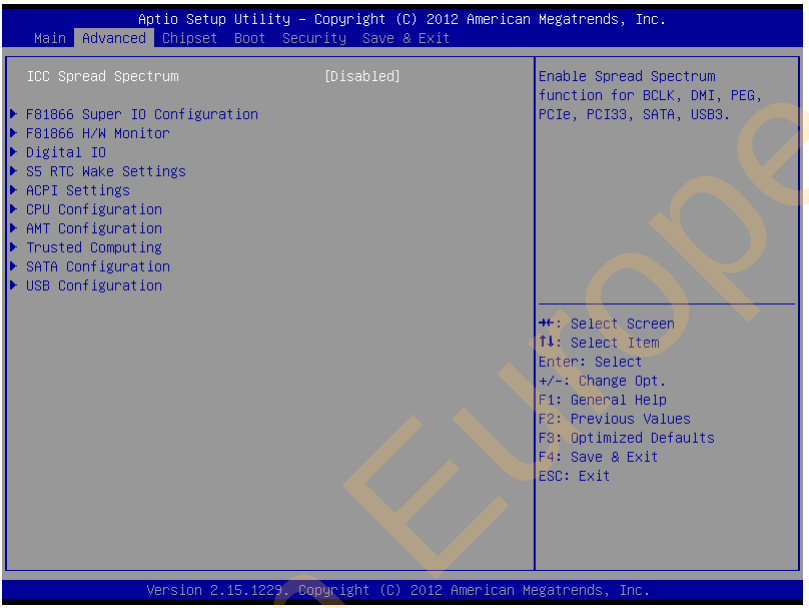
Exit system setup after saving the changes.

Setup Menu

Setup submenu: Main



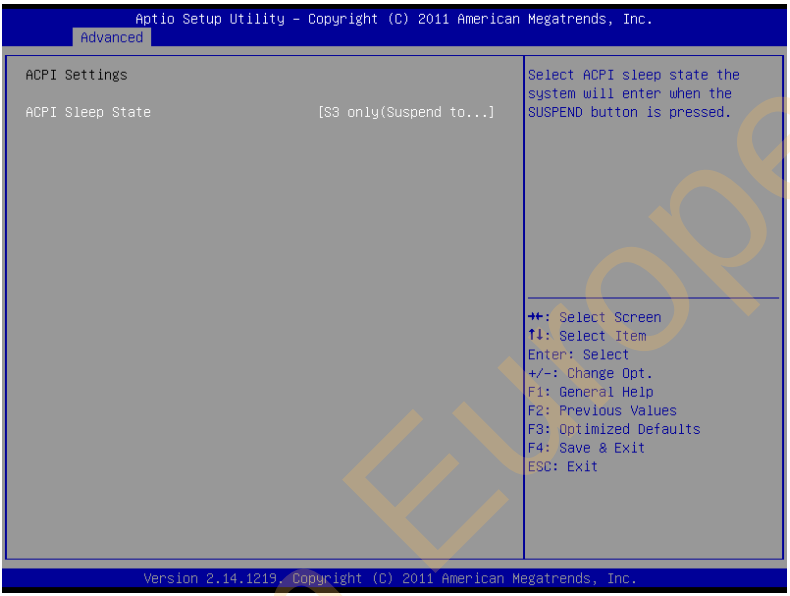
Setup submenu: Advanced



Options summary:

ICC Spread Spectrum	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable Spread Spectrum function for BCLK, DMI, PEG, PCIe, PCI33, SATA, USB3.		

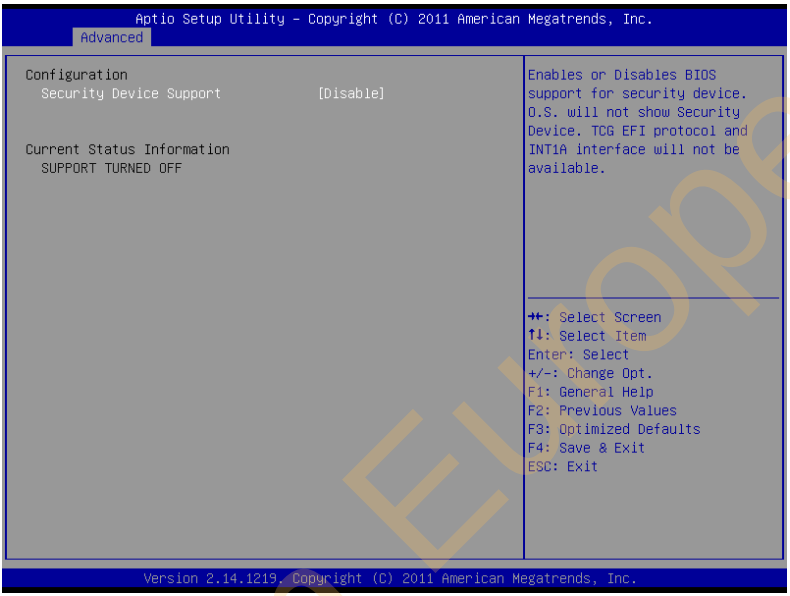
ACPI Settings



Options summary:

Suspend mode	S1 only (CPU Stop Clock)	
	S3 only (Suspend to RAM)	Optimal Default, Failsafe Default
Select the ACPI state used for System Suspend		

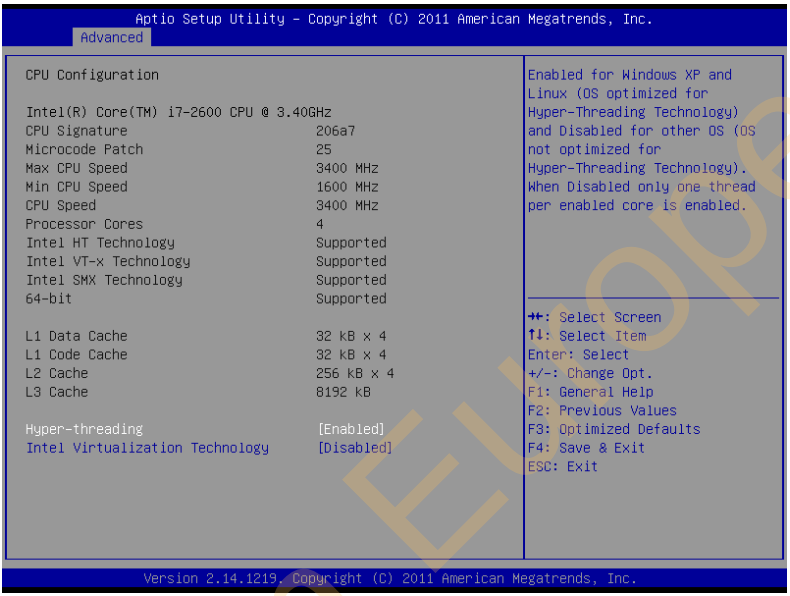
Trusted Computing



Options summary:

Security Device Support	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		

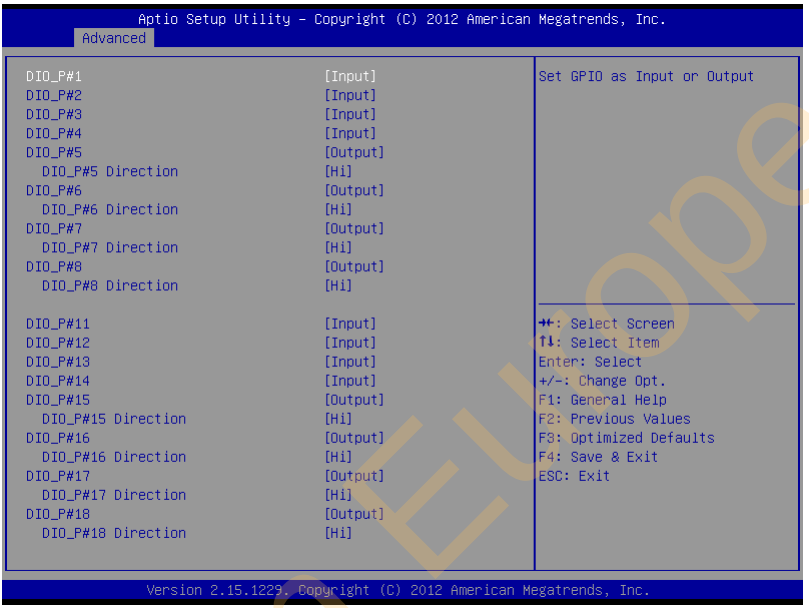
CPU Configuration



Options summary:

Hyper-Threading	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable CPU Hyper-Threading function		
Intel Virtualization Technology	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology		

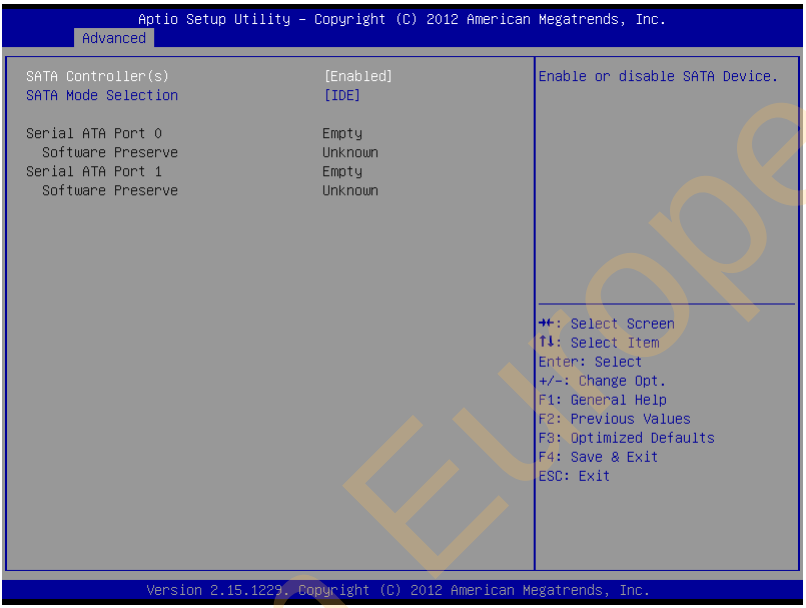
Digital IO



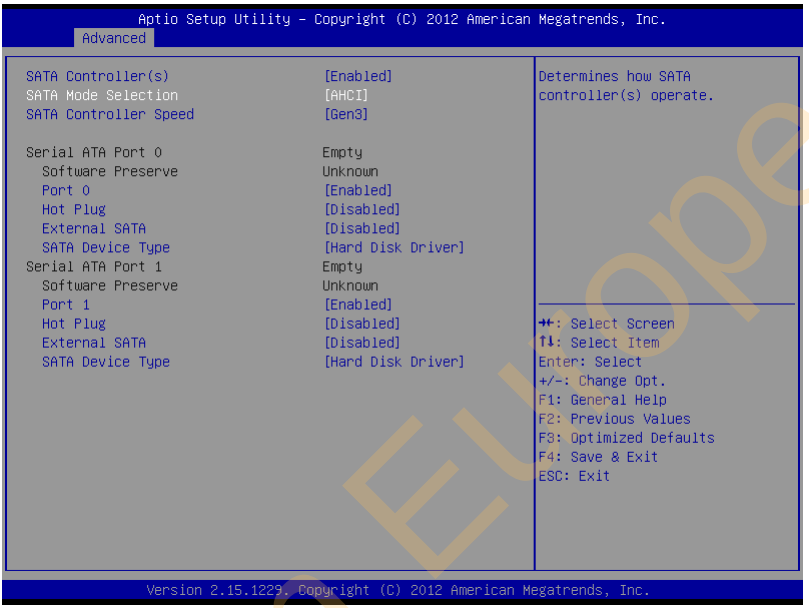
Options summary:

DIO_P#1~4	Input	Default
	Output	
Allows BIOS to select input/output function to corresponding DIO ping.		
DIO_P#5~8	Input	
	Output	Default
Allows BIOS to select input/output function to corresponding DIO ping.		
DIO_P#5~8 Direction	Low	
	Hi	Default
Allows BIOS to select high/low voltage level to output to corresponding DIO ping.		
DIO_P#11~14	Input	Default
	Output	
Allows BIOS to select input/output function to corresponding DIO ping.		
DIO_P#15~18	Input	
	Output	Default
Allows BIOS to select input/output function to corresponding DIO ping.		
DIO_P#15~18 Direction	Low	
	Hi	Default
Allows BIOS to select high/low voltage level to output to corresponding DIO ping.		

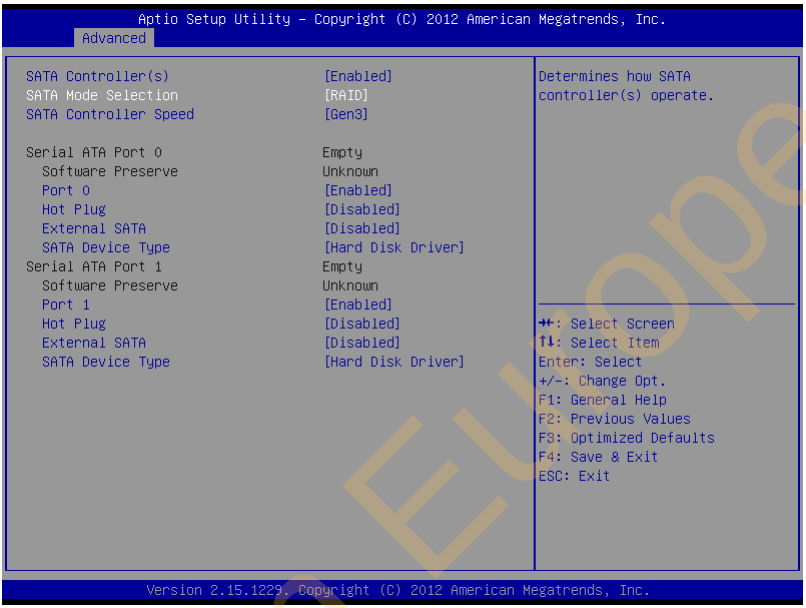
IDE Configuration (IDE)



IDE Configuration (AHCI)



IDE Configuration (RAID)



Options summary:

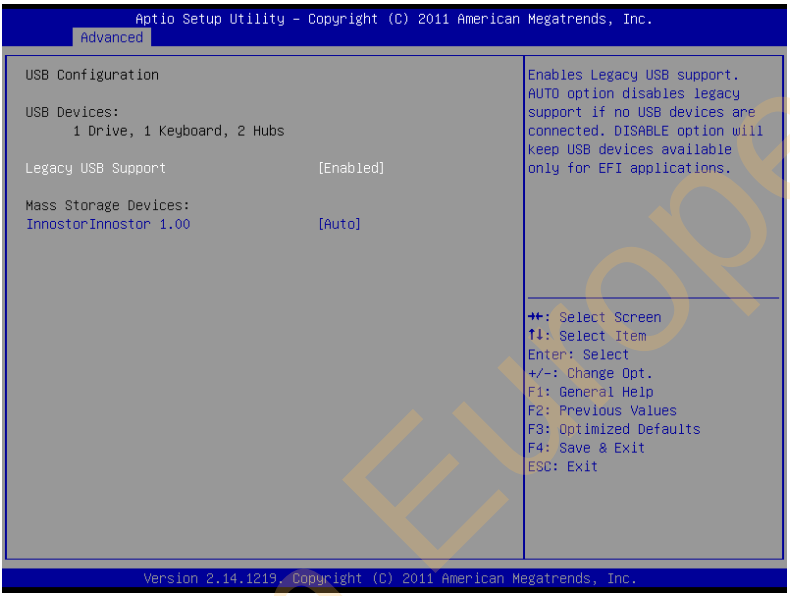
SATA Controllers	Disabled	
	Enabled	Default
En/Disable SATA Controller.		
SATA Mode	IDE	Default
	AHCI	
	RAID	
IDE: Configure SATA controllers as legacy IDEAHCI: Configure SATA controllers to operate in AHCI mode		
SATA Controller Speed	Gen1	
	Gen2	
	Gen3	Default
Indicates the maximum speed the SATA controller can support.		
Port x	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable SATA Port.		
Hot Plug	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable Hot Plug feature.		

AMT Configuration

Options summary:

Intel AMT	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable Intel Active Management Technology BIOS Extension. Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.		
Un-configure ME	Disabled	Optimal Default, Failsafe Default
	Enabled	
OEMFlag Bit 15: Un-Configure ME without password.		

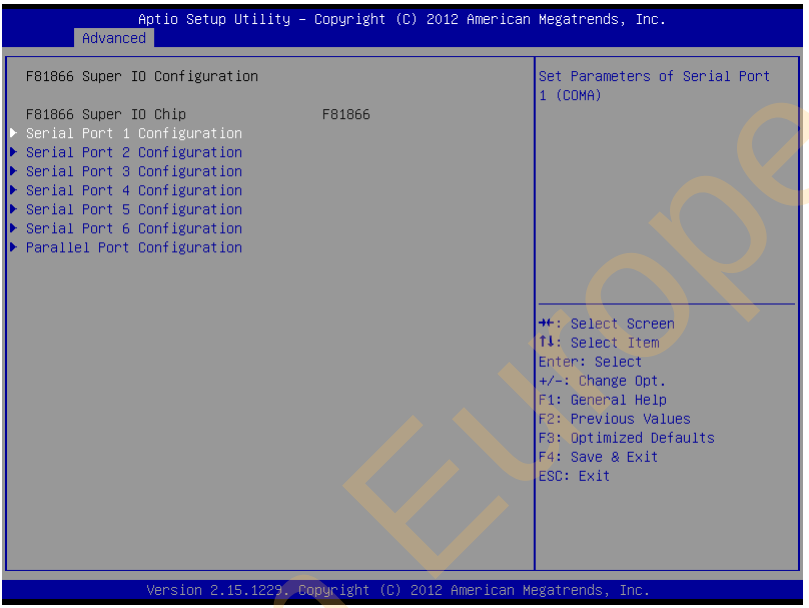
USB Configuration



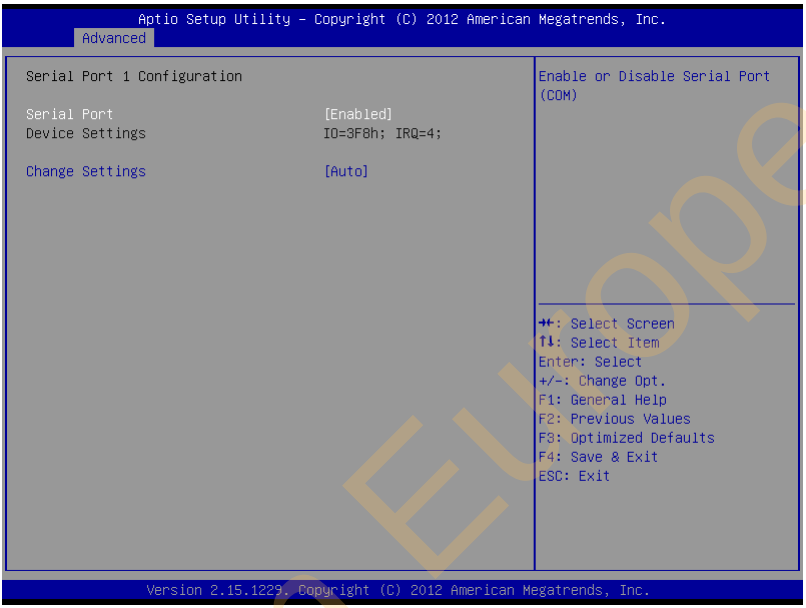
Options summary:

Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		
Device Name (Emulation Type)	Auto	Optimal Default, Failsafe Default
	Floppy	
	Forced FDD	
	Hard Disk	
	CDROM	
If Auto. USB devices less than 530MB will be emulated as Floppy and remaining as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD(Ex. ZIP drive)		

F81866 Super IO Configuration



Serial Port 1 Configuration



Options summary:

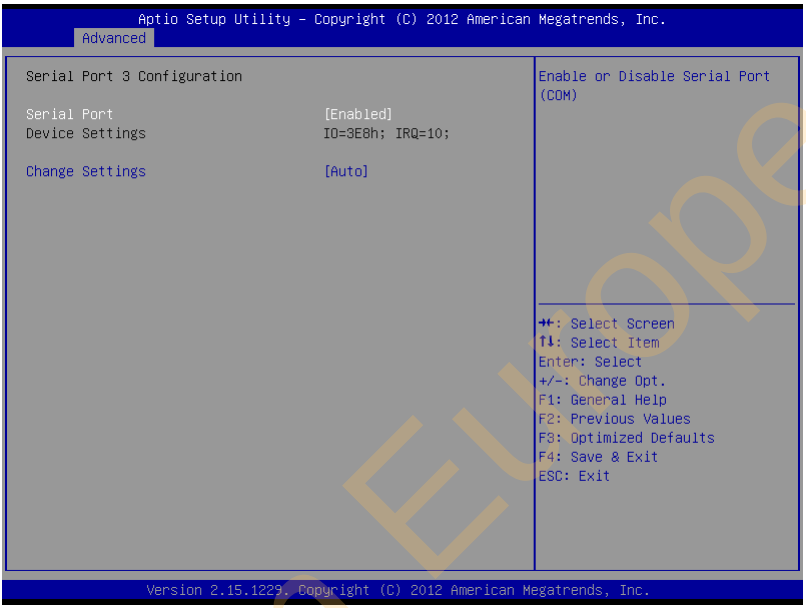
Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Change Settings	Auto	Default
	IO=3F8h; IRQ=4;	
	IO=3F8h; IRQ=3,4;	
	IO=2F8h; IRQ=3,4;	
	IO=3E8h; IRQ=3.4	
	IO=2E8h; IRQ=3,4;	
Allows BIOS to Select Serial Port resource.		

Serial Port 2 Configuration

Options summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Device Mode	RS232	Default
	RS422	
	RS485	
Select working model.		
Change Settings	Auto	Default
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=3,4;	
	IO=2F8h; IRQ=3,4;	
	IO=3E8h; IRQ=3,4;	
	IO=2E8h; IRQ=3,4;	
Allows BIOS to Select Serial Port resource.		

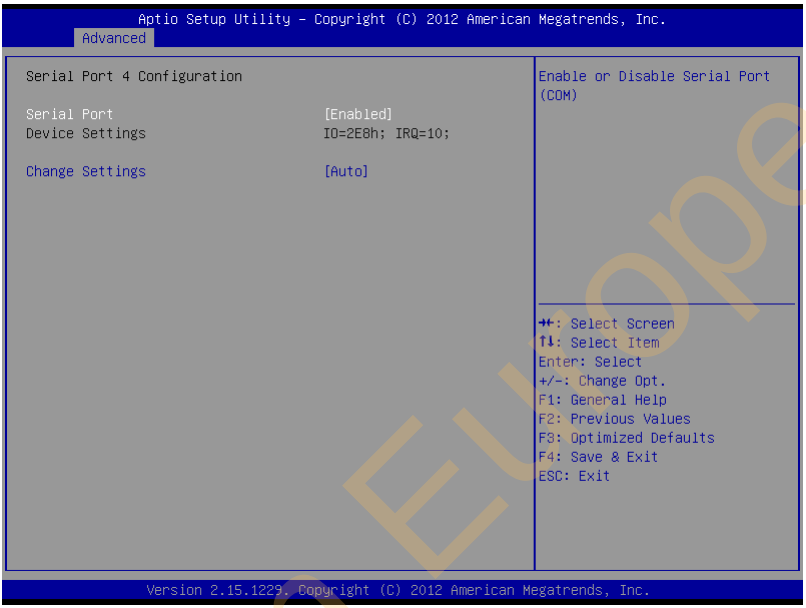
Serial Port 3 Configuration



Options summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Change Settings	Auto	Default
	IO=3E8h; IRQ=10;	
	IO=3E8h; IRQ=10,11;;	
	IO=2E8h; IRQ=10,11;	
	IO=2D0h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11;	
Allows BIOS to Select Serial Port resource.		

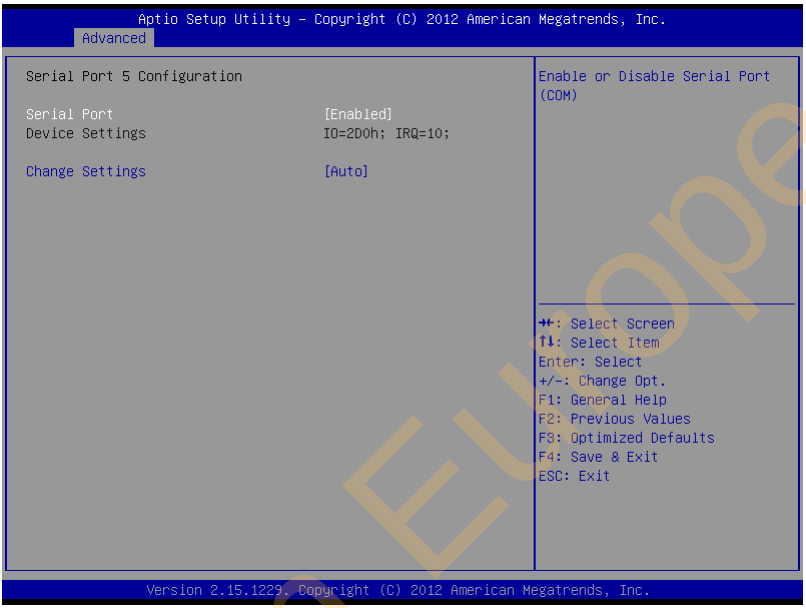
Serial Port 4 Configuration



Options summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Change Settings	Auto	Default
	IO=2E8h; IRQ=10;	
	IO=3E8h; IRQ=10,11;;	
	IO=2E8h; IRQ=10,11;	
	IO=2D0h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11;	
Allows BIOS to Select Serial Port resource.		

Serial Port 5 Configuration



Options summary:

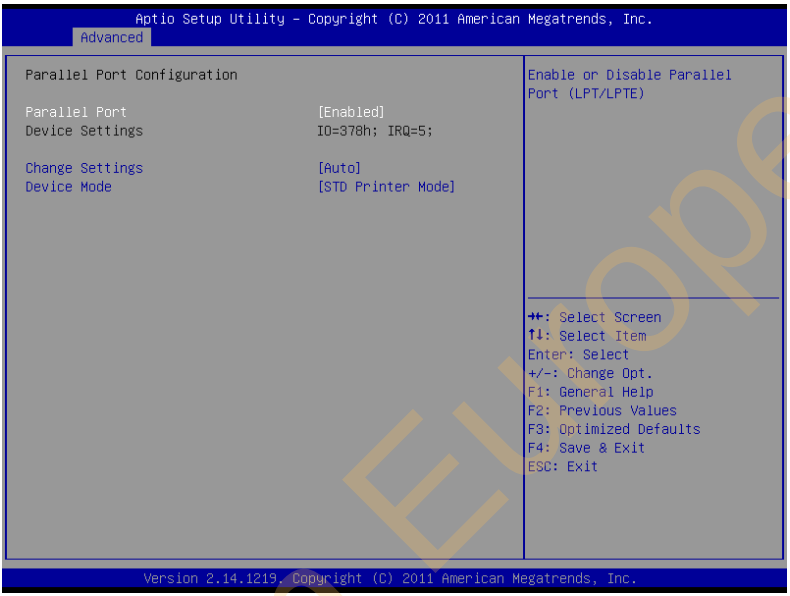
Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Device Mode	RS232	Default
	RS422	
	RS485	
Select working model.		
Change Settings	Auto	Default
	IO=2D0h; IRQ=10;	
	IO=3E8h; IRQ=10,11;;	
	IO=2E8h; IRQ=10,11;	
	IO=2D0h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11;	
Allows BIOS to Select Serial Port resource.		

Serial Port 6 Configuration

Options summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable correspond serial port.		
Device Mode	RS232	Default
	RS422	
	RS485	
Select working model.		
Change Settings	Auto	Default
	IO=2D8h; IRQ=10;	
	IO=3E8h; IRQ=10,11;;	
	IO=2E8h; IRQ=10,11;	
	IO=2D0h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11;	
Allows BIOS to Select Serial Port resource.		

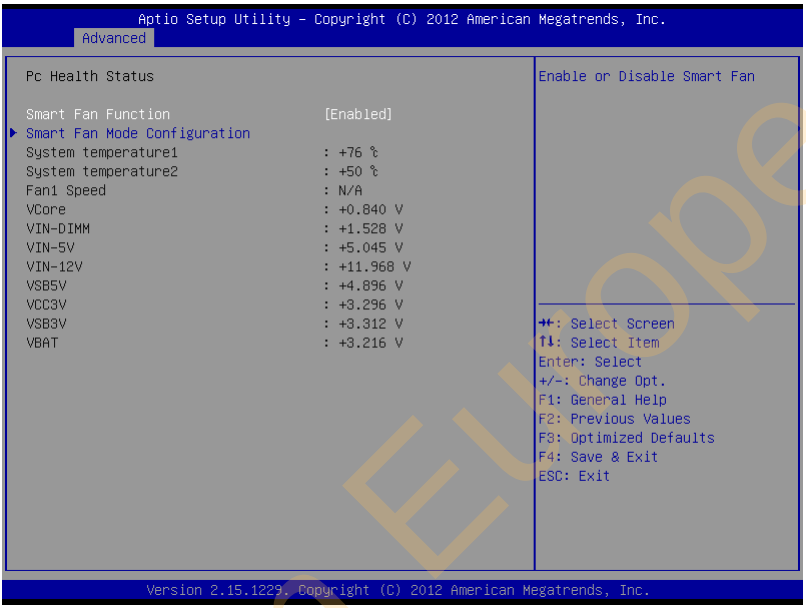
Parallel Port Configuration



Options summary:

Parallel Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable Parallel port.		
Change Settings (Parallel Port)	Auto	Default
	IO=378h; IRQ=5;	
	IO=378h; IRQ=5,7;	
	IO=278h; IRQ=5,7;	
	IO=3BCh; IRQ=5,7;	
Allows BIOS to Select Serial Port resource.		
Device Mode	STD Printer Mode	Default
	SPP Mode	
	EPP-1.9 and SPP Mode	
	EPP-1.9 and SPP Mode	
	ECP Mode	
	ECP and EPP 1.9 Mode	
	ECP and EPP 1.7 Mode	
Change the Printer Port mode.		

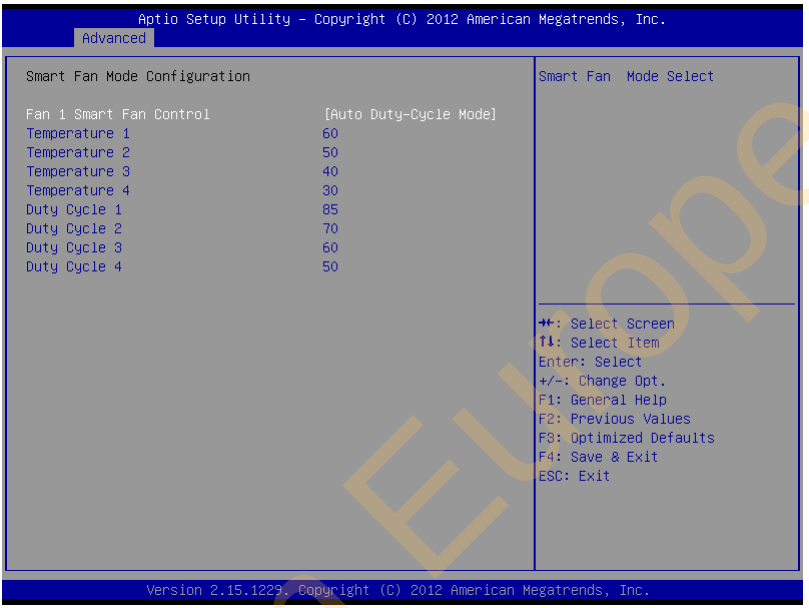
F81866 H/W Monitor



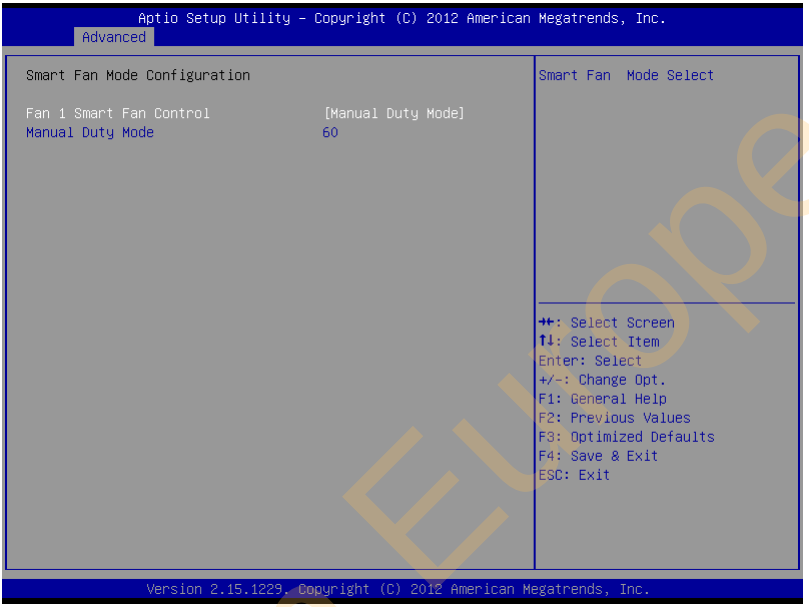
Options summary:

Smart Fan Function	Disabled	
	Enabled	Default
Enable or Disable Smart Fan.		

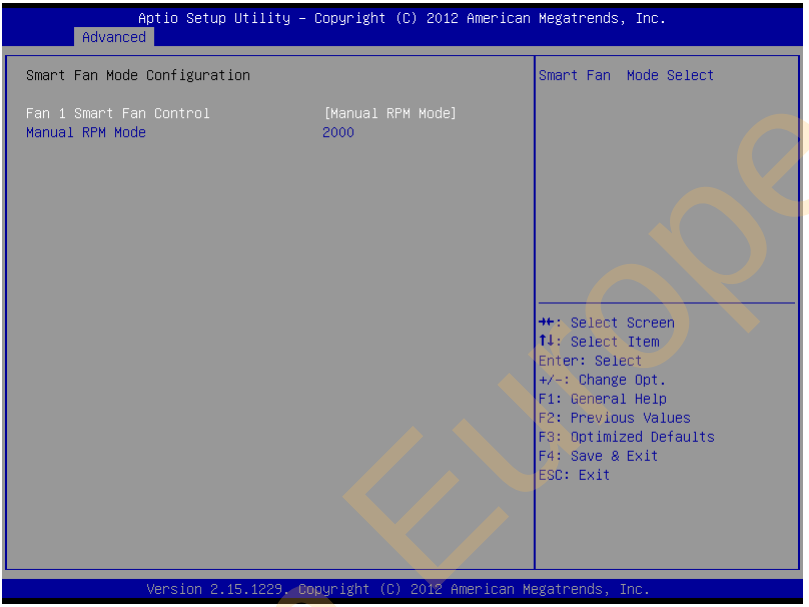
Smart Fan Mode Configuration (Auto Duty-Cycle Mode)



Smart Fan Mode Configuration (Manual Duty Mode)



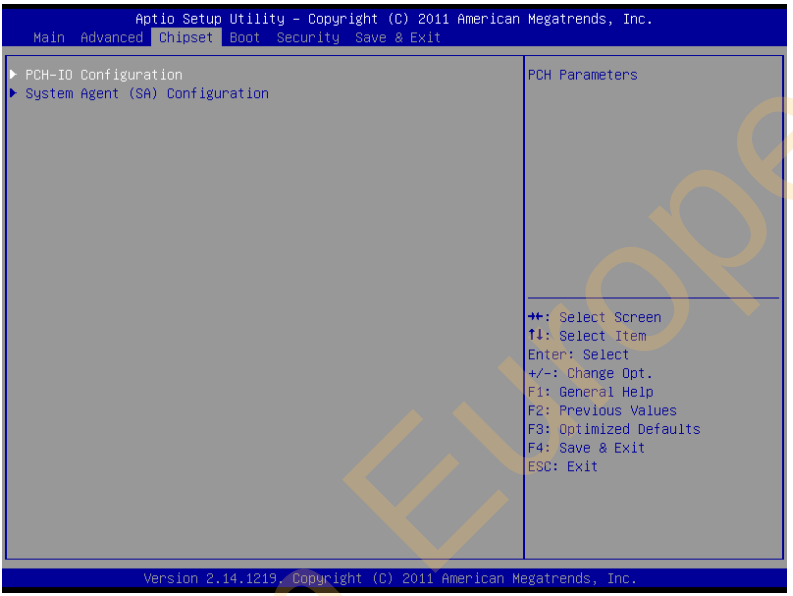
Smart Fan Mode Configuration (Manual RPM Mode)



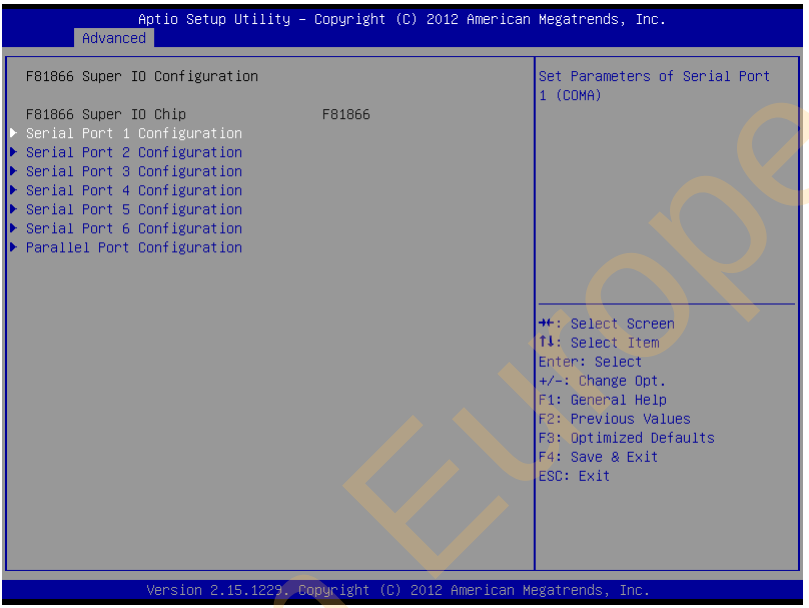
Options summary:

Fan 1 Smart Fan Control	Manual Duty Mode	
	Auto RPM Mode	
	Auto Duty-Cycle Mode	Default
Smart Fan Mode Select		
Temperature 1	60	Default
Temperature 2	50	Default
Temperature 3	40	Default
Temperature 4	30	Default
Duty Cycle 1	85	Default
Duty Cycle 2	70	Default
Duty Cycle 3	60	Default
Duty Cycle 4	50	Default
Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100.		
Manual RPM Mode	2000	Default
Manual mode fan control, user can write expected RPM count 500-10000		
Manual Duty Mode	60	Default
Manual mode fan control, user can write expected duty cycle (PWM fan type)1-100		

Setup submenu: Chipset



PCH-IO Configuration

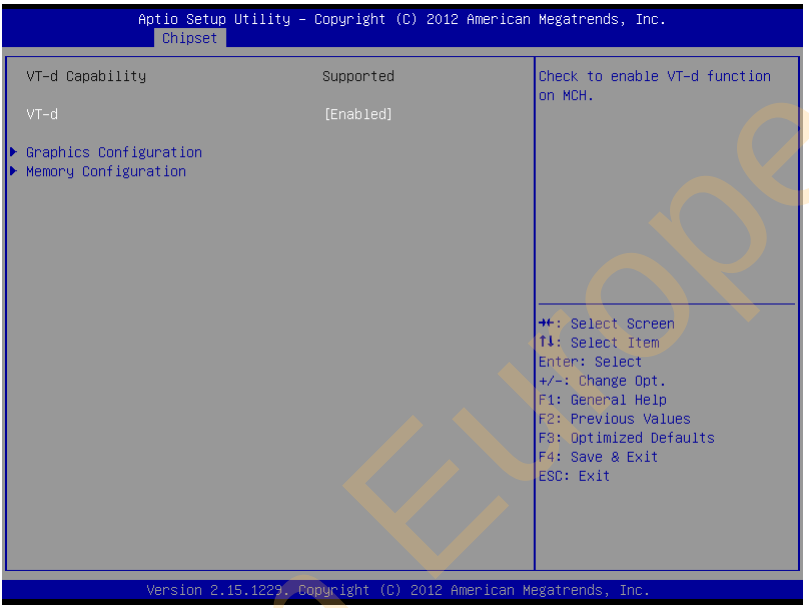


Options summary:

Mini Card2 Controller	Disabled	
	Enabled	Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Default
	Gen1	
	Gen2	
Select PCI Express port speed.		
Mini Card1 Controller	Disabled	
	Enabled	Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Default
	Gen1	
	Gen2	
Select PCI Express port speed.		
PCH LAN Controller	Disabled	
	Enabled	Default
Control the PCI Express Root Port.		
I82583V LAN Controller	Disabled	

	Enabled	Default
Control the PCI Express Root Port		
Azalia	Disabled	
	Enabled	
	Auto	Default
Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled; Enabled = Azalia will be unconditionally enabled; Auto = Azalia will be enabled if present, disabled otherwise.		
Azalia Internal HDMI Codec	Disabled	
	Enabled	Default
Enable or disable internal HDMI codec for Azalia.		
Power Mode	ATX Type	Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Always OFF	
	Always ON	
	Last State	Default
Select AC power state when power is re-applied after a power failure.		
Resume On Ring	Disabled	
	Enabled	Default
Enable/Disable Resume from RI# signal.		

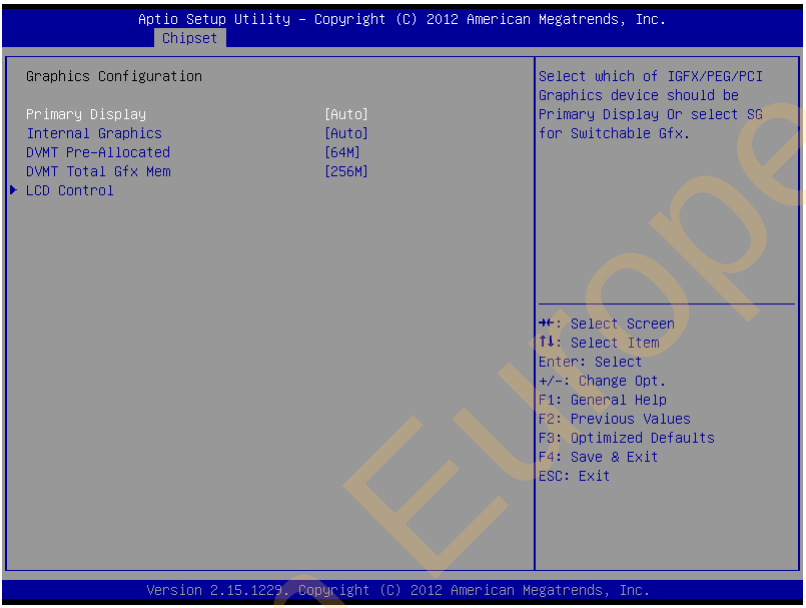
System Agent (SA) Configuration



Options summary:

VT-d	Disabled	
	Enabled	Default
Check to enable VT-d function on MCH		

Graphics Configuration



Options summary:

Primary Display	Auto	Default
	IGFX	
	PEG	
	PCI	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select SG for Switchable Gfx.		
Internal Graphics	Auto	Default
	Disabled	
	Enabled	
Keep IGD enabled based on setup options.		

DVMT Pre-Allocated	32MB	Default
	64MB	
	96MB	
	128MB	
	160MB	
	192MB	
	224MB	
	256MB	
	288MB	
	320MB	
	352MB	
	384MB	
	416MB	
	448MB	
	480MB	
	512MB	
	1024MB	
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.		
DVMT Total Gfx Mem	128MB	Default
	256MB	
	MAX	
Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.		

LCD Control

Options summary:

Primary Display	VBIOS Default	Default
	CRT	
	DVI	
	LVDS	
	HDMI	
Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear base on your selection. VGA modes will be supported only on primary display.		
Active LFP	No LVDS	Default
	Internal –LVDS	
	External -LVDS	
Select the active LFP Configuration. No LVDS: VBIOS does not enable LVDS. Internal-LVDS:VBIOS enables LVDS driver by Integrated encoder. External-LVDS:LFP Driven by PTN-3460		

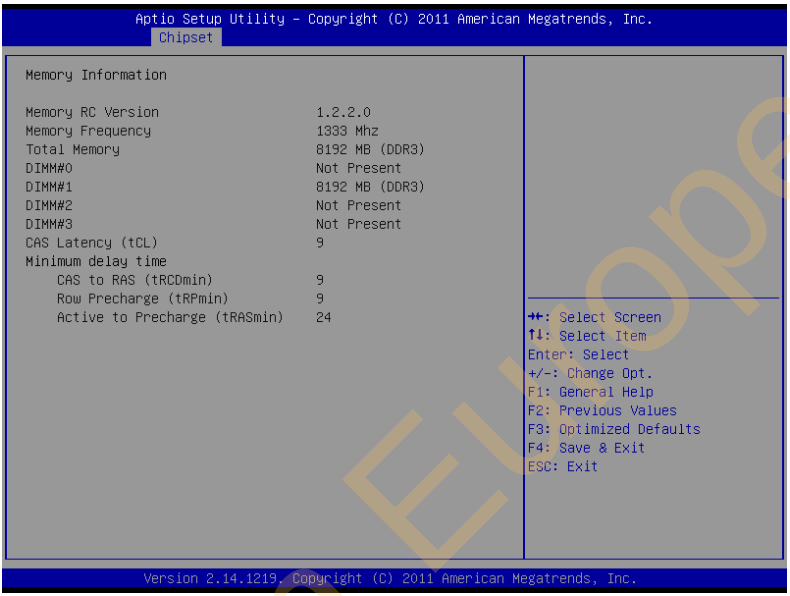
Internal-LVDS

LCD Panel Type	640x 480 18Bit	
	800x 480 18Bit	
	800x 600 18Bit	
	1024x 768 18Bit	Default
	1024x 768 24Bit	
	1280x 768 24Bit	
	1280x102414Bit	
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		

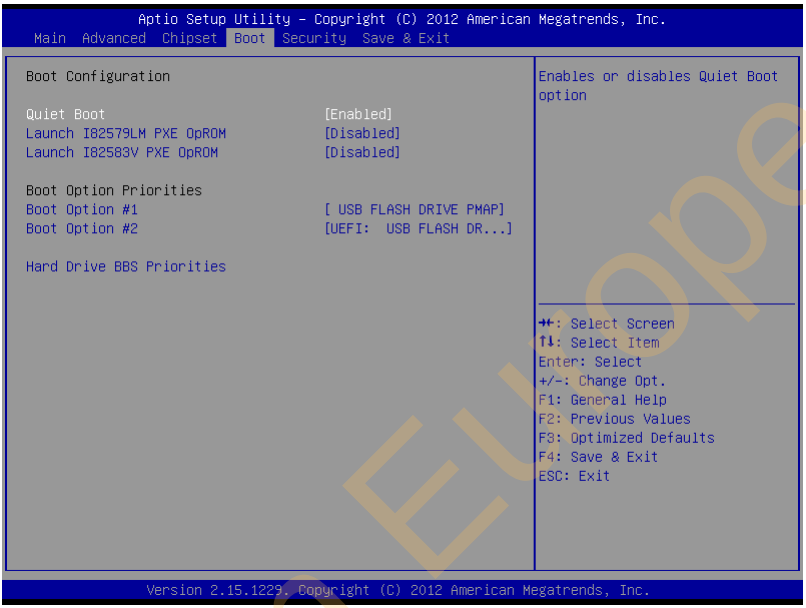
External-LVDS

LCD Panel Type	1600x1200 48Bit (Ext. Only)	Default
	1920x1080 48Bit (Ext. Only)	
	1920x1200 48Bit (Ext. Only)	
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		
Backlight Control	PWM Inverted	Default
	PWM Normal	
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		
LVDS1 Backlight Level	100%	
	90%	
	80%	
	70%	Default
	60%	
	50%	
	40%	
	30%	
	20%	
	10%	
	0%	
Select Backlight brightness of LVDS		

Memory Information



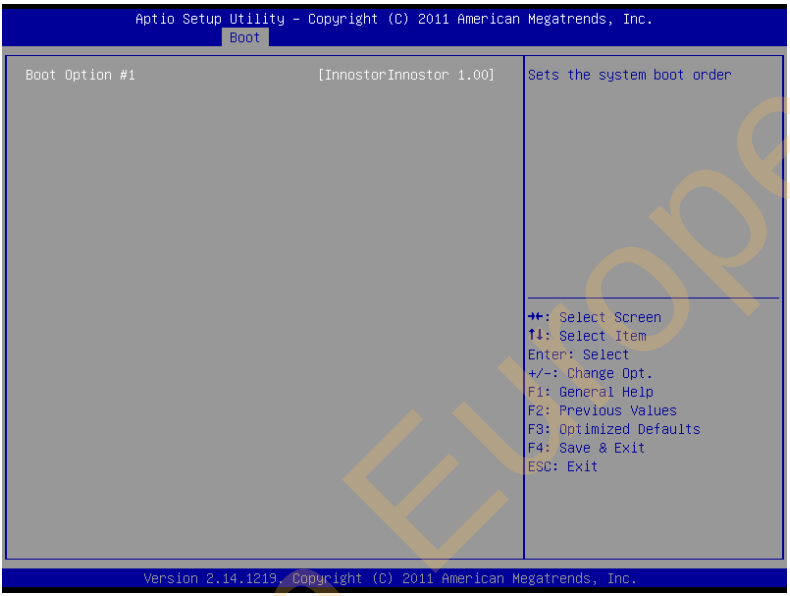
Setup submenu: Boot



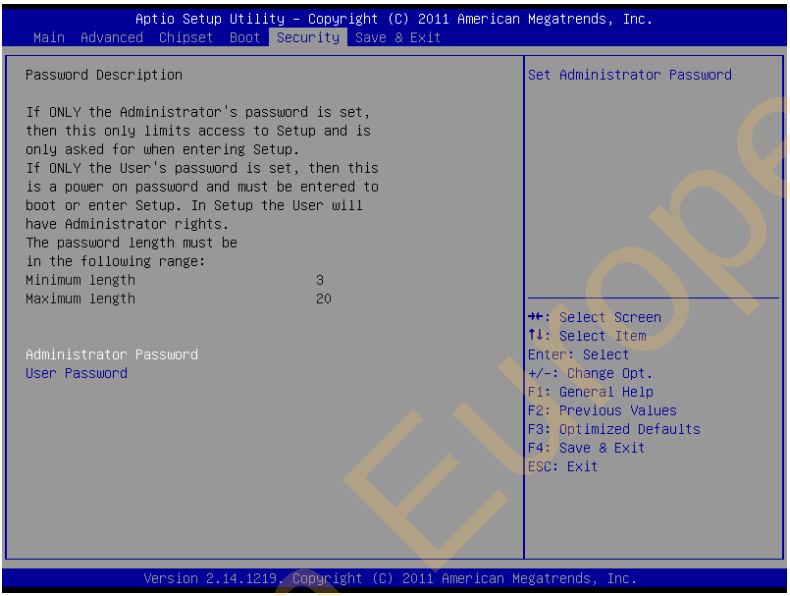
Options summary:

Quiet Boot	Disabled	
	Enabled	Default
En/Disable showing boot logo.		
Launch I82579LM PXE OpROM	Disabled	Default
	Enabled	
En/Disable Legacy Boot Option for I82579LM.		
Launch I82583V PXE OpROM	Disabled	Default
	Enabled	
En/Disable Legacy Boot Option for I82583V.		

BBS Priorities



Security



Change User/Supervisor Password

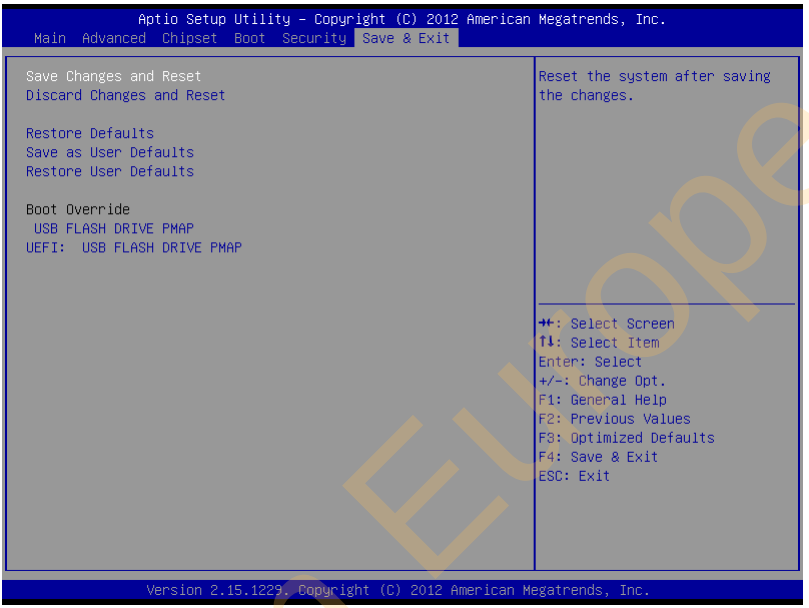
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

Setup submenu: Exit



Chapter 4

Driver Installation

The EPIC-QM77 comes with a DVD-ROM that contains all drivers and utilities that meet your needs.

Follow the sequence below to install the drivers:

Step 1 – Install Chipset Driver

Step 2 – Install VGA Driver

Step 3 – Install LAN (Intel_82579) Driver

Step 4 – Install Audio Driver

Step 5 – Install ME Driver

Step 6 – Install RAID & AHCI Driver

Step 7 – Install TPM Driver

Step 8 – Install Touch Driver

Step 9 – Install USB3.0 Driver

Please read instructions below for further detailed installations.

4.1 Installation:

Insert the EPIC-QM77 DVD-ROM into the DVD-ROM Drive. And install the drivers from Step 1 to Step 9 in order.

Step 1 – Install Chipset Driver

1. Click on the ***Step1 - CHIPSET*** folder and then double click on the ***infinst_autol.exe***
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Step 2 – Install VGA Driver

1. Click on the ***STEP2-VGA*** folder and select the OS folder your system is
2. Double click on the ***Setup.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Note 1:

- This motherboard supports VGA and LVDS display devices. In Single Display mode, use the hot keys to switch between VGA to LVDS device or vice versa. By default, press **<Ctrl>+<Alt>+<F1>** to switch to VGA device and press **<Ctrl>+<Alt>+<F3>** to switch to LVDS device.
- Before removing the current display device, connect the display device that you want to use, and then press the hot keys to switch to that device.

Note 2: If the OS is Windows® XP, you have to install the driver of dotNet Framework first. Simply click on ***dotnetfx35.exe*** located in ***dotNet Framwork*** folder.

Step 3 – Install LAN (Intel_82579) Driver

1. Click on the ***STEP3-LAN (Intel_82579)*** folder and select the OS folder your system is
2. Double click on the ***.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 4 – Install Audio Driver

1. Click on the ***STEP4-AUDIO*** folder and select the OS folder your system is
2. Double click on the ***Setup.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 5 – Install ME Driver

1. Click on the ***STEP5-ME SW*** folder and select the OS folder your system is
2. Double click on the Setup.exe file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 6 – Install RAID & AHCI Driver

Please refer to Appendix D RAID & AHCI Settings

Step 7 – Install TPM Driver

1. Click on the ***STEP7-TPM*** folder and select the OS folder your system is
2. Double click on the ***Setup.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 8 –Install Touch Driver

1. Click on the ***STEP8-TOUCH*** folder and select the appropriate version folder
2. Double click on the ***Setup.exe*** file located in each version folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 9 –Install USB3.0 Driver

1. Click on the ***STEP9-USB3.0*** folder and select the OS folder your system is
2. Double click on the ***Setup.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Appendix

A

Programming the Watchdog Timer

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	**Note**
Index	**0x2E**(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	**0x2F**(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	**Register**	**BitNum**	**Value**	**Note**
Timer Counter	**0x07**(Note3)	**0xF6**(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	**0x07**(Note5)	**0xF5**(Note6)	**3**(Note7)	**0**(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	**0x07**(Note9)	**0xF5**(Note10)	**5**(Note11)	**1**(Note12)	0: Disable 1: Enable
Timeout Status	**0x07**(Note13)	**0xF5**(Note14)	**6**(Note15)	**1**	1: Clear timeout status
Output Mode	**0x07**(Note16)	**0xF5**(Note17)	**4**(Note18)	**1**(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	**0x07**(Note20)	**0xFA**(Note21)	**0**(Note22)	**1**(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

```
**********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN    //This parameter is represented from Note3
#define byte   TimerReg    //This parameter is represented from Note4
#define byte   TimerVal    // This parameter is represented from Note24
#define byte   UnitLDN     //This parameter is represented from Note5
#define byte   UnitReg     //This parameter is represented from Note6
#define byte   UnitBit     //This parameter is represented from Note7
#define byte   UnitVal     //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
#define byte   ModeLDN     // This parameter is represented from Note16
#define byte   ModeReg     // This parameter is represented from Note17
#define byte   ModeBit     // This parameter is represented from Note18
#define byte   ModeVal     // This parameter is represented from Note19
#define byte   WDTRstLDN   // This parameter is represented from Note20
#define byte   WDTRstReg   // This parameter is represented from Note21
#define byte   WDTRstBit   // This parameter is represented from Note22
#define byte   WDTRstVal   // This parameter is represented from Note23
**********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*********************************************************************************
```

```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable (){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig (){
        // Disable WDT counting
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
        // Clear Watchdog Timeout Status
        WDTClearTimeoutStatus();
        // WDT relative parameter setting
        WDTParameterSetting();
}

VOID   WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
        SIOBitSet(LDN, Register, BitNum, Value);
}

VOID   WDTParameterSetting(){
        // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
        // WDT counting unit setting
        SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
        // WDT output mode setting, level / pulse
        SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
        // Watchdog timeout output via WDTRST#
        SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID   WDTClearTimeoutStatus(){
        SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****************************************************************************
```

```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix

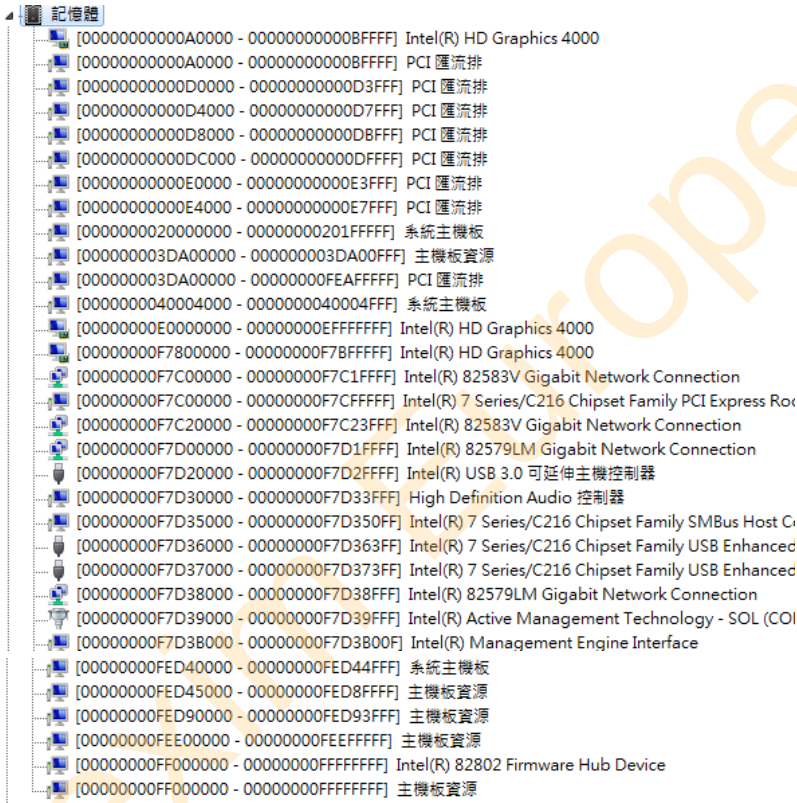
B

I/O Information

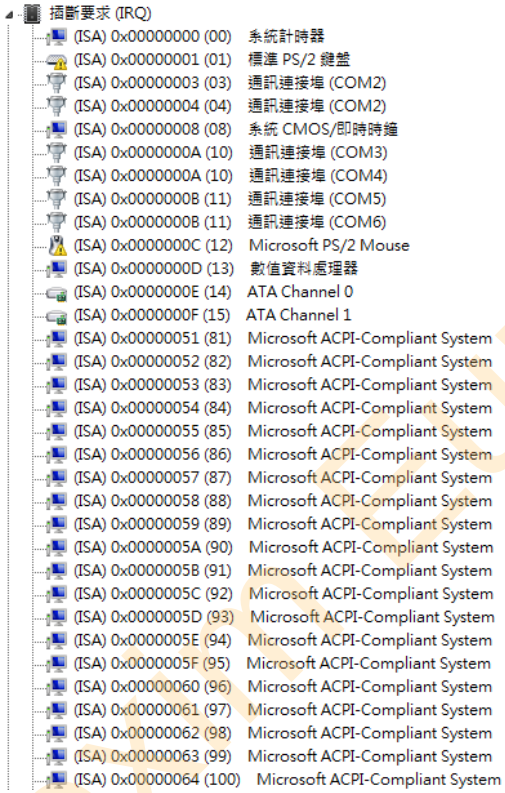
B.1 I/O Address Map

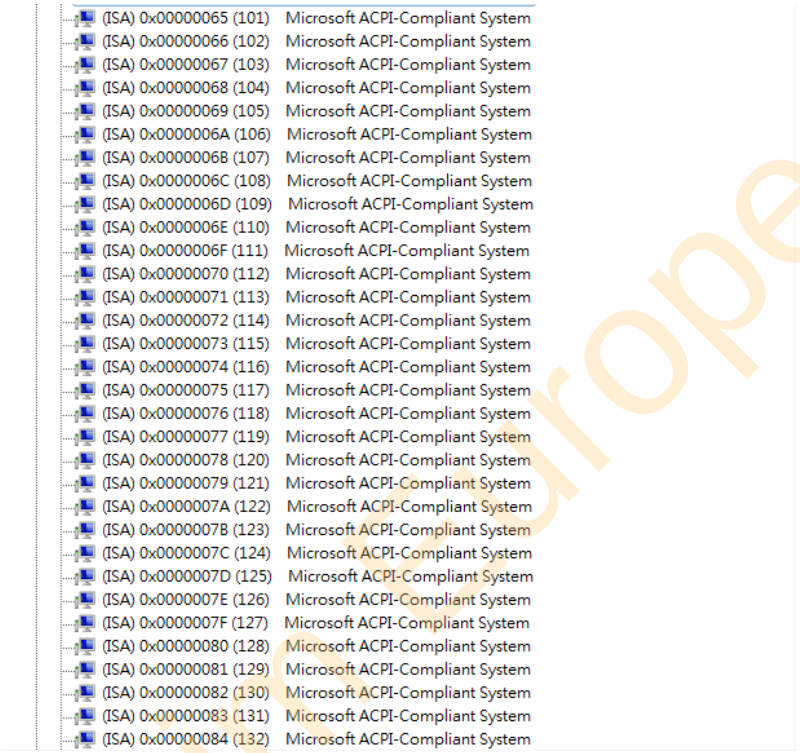
[00000000000000A4 - 00000000000000A5] 可程式插斷控制器
[00000000000000A8 - 00000000000000A9] 可程式插斷控制器
[00000000000000AC - 00000000000000AD] 可程式插斷控制器
[00000000000000B0 - 00000000000000B1] 可程式插斷控制器
[00000000000000B2 - 00000000000000B3] 主機板資源
[00000000000000B4 - 00000000000000B5] 可程式插斷控制器
[00000000000000B8 - 00000000000000B9] 可程式插斷控制器
[00000000000000BC - 00000000000000BD] 可程式插斷控制器
[00000000000000C0 - 00000000000000DF] 直接記憶體存取控制器
[00000000000000E0 - 00000000000000EF] 主機板資源
[00000000000000F0 - 00000000000000FF] 數值資料處理器
[0000000000000170 - 0000000000000177] ATA Channel 1
[00000000000001F0 - 00000000000001F7] ATA Channel 0
[0000000000000290 - 000000000000029F] 主機板資源
[00000000000002D0 - 00000000000002D7] 通訊連接埠 (COM5)
[00000000000002D8 - 00000000000002DF] 通訊連接埠 (COM6)
[00000000000002E8 - 00000000000002EF] 通訊連接埠 (COM4)
[00000000000002F8 - 00000000000002FF] 通訊連接埠 (COM2)
[0000000000000378 - 000000000000037F] 印表機連接埠 (LPT1)
[00000000000003B0 - 00000000000003BB] Intel(R) HD Graphics 4000
[00000000000003C0 - 00000000000003DF] Intel(R) HD Graphics 4000
[00000000000003E8 - 00000000000003EF] 通訊連接埠 (COM3)
[00000000000003F6 - 00000000000003F6] ATA Channel 0
[00000000000003F8 - 00000000000003FF] 通訊連接埠 (COM2)
[0000000000000400 - 0000000000000453] 主機板資源
[0000000000000454 - 0000000000000457] 主機板資源
[0000000000000458 - 000000000000047F] 主機板資源
[00000000000004D0 - 00000000000004D1] 主機板資源
[00000000000004D0 - 00000000000004D1] 可程式插斷控制器
[0000000000000500 - 000000000000057F] 主機板資源
[0000000000000680 - 000000000000069F] 主機板資源
[0000000000000A00 - 0000000000000A0F] 主機板資源
[0000000000000A10 - 0000000000000A1F] 主機板資源
[0000000000000D00 - 0000000000000FFFF] PCI 匯流排
[0000000000001000 - 000000000000100F] 主機板資源
[000000000000164E - 000000000000164F] 主機板資源

B.2 Memory Address Map



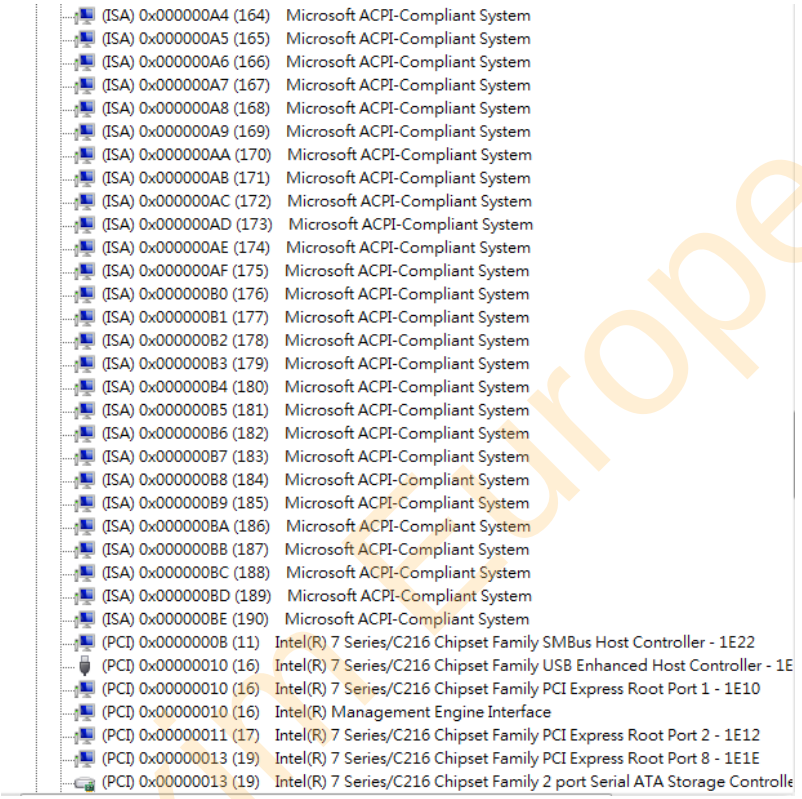
B.3 IRQ Mapping Chart



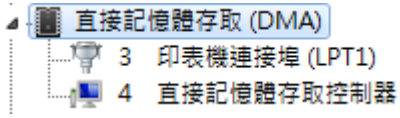


.

(ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
(ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
(ISA) 0x00000087 (135) Microsoft ACPI-Compliant System
(ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
(ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
(ISA) 0x0000008A (138) Microsoft ACPI-Compliant System
(ISA) 0x0000008B (139) Microsoft ACPI-Compliant System
(ISA) 0x0000008C (140) Microsoft ACPI-Compliant System
(ISA) 0x0000008D (141) Microsoft ACPI-Compliant System
(ISA) 0x0000008E (142) Microsoft ACPI-Compliant System
(ISA) 0x0000008F (143) Microsoft ACPI-Compliant System
(ISA) 0x00000090 (144) Microsoft ACPI-Compliant System
(ISA) 0x00000091 (145) Microsoft ACPI-Compliant System
(ISA) 0x00000092 (146) Microsoft ACPI-Compliant System
(ISA) 0x00000093 (147) Microsoft ACPI-Compliant System
(ISA) 0x00000094 (148) Microsoft ACPI-Compliant System
(ISA) 0x00000095 (149) Microsoft ACPI-Compliant System
(ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
(ISA) 0x00000097 (151) Microsoft ACPI-Compliant System
(ISA) 0x00000098 (152) Microsoft ACPI-Compliant System
(ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
(ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
(ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
(ISA) 0x0000009C (156) Microsoft ACPI-Compliant System
(ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
(ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System
(ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
(ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
(ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System
(ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
(ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
(ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System



B.4 DMA Channel Assignments



Appendix

C

Mating Connector

C.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model number		
CN2	Touch Screen Connector	PINREX	710-75-09W001		
CN3	SATA Power Connector	PINREX	721-75-02W001		1702150155
CN5	1st Backlight Connector	CATCH	H732-05		
CN6	2nd Backlight Connector	CATCH	H732-05		
CN9	LPT_DIO Connector	Astron	25-2103-213-1G-R		
CN10	Audio Connector	PINREX	712-75-10W001		1709100254
CN13	Front Panel Connector	PINREX	712-75-10W001		
CN14	Amp R-channel Connector	PINREX	712-75-02W001		
CN16	LPC Connector	CATCH	H746-12		1701260200
CN17	Amp L-channel Connector	PINREX	712-75-02W001		
CN18	3G SIM Connector	ACES	50375-00511-001		
USB3	USB2.0 Connector	PINREX	712-75-05W001		1700050207

USB4	USB2.0 Connector	PINREX	712-75-05W001		1700050207
USB5	USB2.0 Connector	PINREX	712-75-05W001		1700050207
USB6	USB2.0 Connector	PINREX	712-75-05W001		1700050207
COM3	COM3 RS-232 Serial Port Connector	PINREX	712-75-09W001		1701090150
COM4	COM4 RS-232 Serial Port Connector	PINREX	712-75-09W001		1701090150
COM5	COM5 RS-232 Serial Port Connector	PINREX	712-75-09W001		1701090150
COM6	COM6 RS-232 Serial Port Connector	PINREX	712-75-09W001		1701090150
KB1	PS/2 Keyboard Mouse Connector	CATCH	H752-06		1700060155
FAN1	Fan Connector	PINREX	742-75-04W001		
BAT1	RTC Battery Connector	CATCH	2P 1201-700-02S		
LVDS1	1st LVDS Connector	E-call	0109-02-522-300		
LVDS2	2nd LVDS Connector	E-call	0109-02-522-300		

Appendix

D

Electrical Specifications for I/O Ports

D.1 Electrical Specifications for I/O Ports

I/O	Reference	Signal Name	Rate Output
LVDS Port 1	LVDS1	VCC	+3.3V/1A or +5V/1A
LVDS Port 2	LVDS2	VCC	+3.3V/1A or +5V/1A
LPC Port	CN16	+3.3V	+3.3V/0.5A
LVDS Port 1 Inverter / Backlight Connector	CN5	VDD	+5V/2A or +12V/2A
LVDS Port 2 Inverter / Backlight Connector	CN6	VDD	+5V/2A or +12V/2A
+5V Output for SATA HDD	CN3	+5V	+5V/1A
Audio I/O Port	CN10	+5V	+5V/0.5A
2Pin PWRIN (Optional)	CN15	+12V	+12V/3A
ATX 4Pin PWRIN	CN12	+12V	+12V/6A
FAN	FAN1	+5V	+5V/0.5A
Mini Card Slot	CN8	+3.3VSB +1.5V	+3.3V/1A +1.5V/0.375A
mSATA Slot	CN7	+3.3VSB +1.5V	+3.3V/1A +1.5V/0.375A
USB 3.0 Ports 1 and 2	USB1	+5VSB	+5V/1A (per channel)
USB 2.0 Ports 3.4.5.6	USB3/USB4 USB5/USB6	+5VSB	+5V/0.5A (per channel)
COM Port 2	COM1B	+5V/+12V	+5V/1A or +12V/1A
Digital IO Port	CN9	GPIO0~GPIO15	+5V (Ext. Pull Up)
VGA / DVI Ports	CN1	VGA: +5V DVI : +5V	+5V/0.5A

D.2 DIO Programming

EPIC-QM77 utilizes FINTEK 81866 chipset as its Digital I/O controller.

Below are the procedures to complete its configuration and the AAEON initial watchdog timer program is also attached based on which you can develop customized program to fit your application.

There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.(These three steps are the same as programming WDT)

D.3 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	**Note**
Index	**0x2E**(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	**0x2F**(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	**Register**	**BitNum**	**Value**	**Note**
DIO-1 Pin Status	**0x06**(Note3)	**0x82**(Note4)	**0**(Note5)		PE
DIO-2 Pin Status	**0x06**(Note6)	**0x82**(Note7)	**1**(Note8)		BUSY
DIO-3 Pin Status	**0x06**(Note9)	**0x82**(Note10)	**2**(Note11)		ACK#
DIO-4 Pin Status	**0x06**(Note12)	**0x82**(Note13)	**3**(Note14)		SLIN#
DIO-5 Pin Status	**0x06**(Note15)	**0x82**(Note16)	**4**(Note17)		PINIT#
DIO-6 Pin Status	**0x06**(Note18)	**0x82**(Note19)	**5**(Note20)		ERR#
DIO-7 Pin Status	**0x06**(Note21)	**0x82**(Note22)	**6**(Note23)		AFD#
DIO-8 Pin Status	**0x06**(Note24)	**0x82**(Note25)	**7**(Note26)		STB#
DIO-11 Pin Status	**0x06**(Note3-1)	**0x8A**(Note4-1)	**0**(Note5-1)		PD0
DIO-12 Pin Status	**0x06**(Note6-1)	**0x8A**(Note7-1)	**1**(Note8-1)		PD1
DIO-13 Pin Status	**0x06**(Note9-1)	**0x8A**(Note10-1)	**2**(Note11-1)		PD2
DIO-14 Pin Status	**0x06**(Note12-1)	**0x8A**(Note13-1)	**3**(Note14-1)		PD3
DIO-15 Pin Status	**0x06**(Note15-1)	**0x8A**(Note16-1)	**4**(Note17-1)		PD4
DIO-16 Pin Status	**0x06**(Note18-1)	**0x8A**(Note19-1)	**5**(Note20-1)		PD5
DIO-17 Pin Status	**0x06**(Note21-1)	**0x8A**(Note22-1)	**6**(Note23-1)		PD6
DIO-18 Pin Status	**0x06**(Note24-1)	**0x8A**(Note25-1)	**7**(Note26-1)		PD7

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0x88(Note28)	0(Note29)	(Note30)	PE
DIO-2 Output Data	0x06(Note31)	0x88(Note32)	1(Note33)	(Note34)	BUSY
DIO-3 Output Data	0x06(Note35)	0x88(Note36)	2(Note37)	(Note38)	ACK#
DIO-4 Output Data	0x06(Note39)	0x88(Note40)	3(Note41)	(Note42)	SLIN#
DIO-5 Output Data	0x06(Note43)	0x88(Note44)	4(Note45)	(Note46)	PINIT#
DIO-6 Output Data	0x06(Note47)	0x88(Note48)	5(Note49)	(Note50)	ERR#
DIO-7 Output Data	0x06(Note51)	0x88(Note52)	6(Note53)	(Note54)	AFD#
DIO-8 Output Data	0x06(Note55)	0x88(Note56)	7(Note57)	(Note58)	STB#
DIO-11 Output Data	0x06(Note27-1)	0x89(Note28-1)	0(Note29-1)	(Note30-1)	PD0
DIO-22 Output Data	0x06(Note31-1)	0x89(Note32-1)	1(Note33-1)	(Note34-1)	PD1
DIO-13 Output Data	0x06(Note35-1)	0x89(Note36-1)	2(Note37-1)	(Note38-1)	PD2
DIO-14 Output Data	0x06(Note39-1)	0x89(Note40-1)	3(Note41-1)	(Note42-1)	PD3
DIO-15 Output Data	0x06(Note43-1)	0x89(Note44-1)	4(Note45-1)	(Note46-1)	PD4
DIO-16 Output Data	0x06(Note47-1)	0x89(Note48-1)	5(Note49-1)	(Note50-1)	PD5
DIO-17 Output Data	0x06(Note51-1)	0x89(Note52-1)	6(Note53-1)	(Note54-1)	PD6
DIO-18 Output Data	0x06(Note55-1)	0x89(Note56-1)	7(Note57-1)	(Note58-1)	PD7

D.4 Digital I/O Sample Program

```
**********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte    SIOIndex    //This parameter is represented from Note1
#define byte    SIOData     //This parameter is represented from Note2
#define   void    IOWriteByte(byte IOPort, byte Value);
#define   byte    IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte    DInput1LDN    // This parameter is represented from Note3
#define byte    DInput1Reg    // This parameter is represented from Note4
#define byte    DInput1Bit    // This parameter is represented from Note5
#define byte    DInput2LDN    // This parameter is represented from Note6
#define byte    DInput2Reg    // This parameter is represented from Note7
#define byte    DInput2Bit    // This parameter is represented from Note8
#define byte    DInput3LDN    // This parameter is represented from Note9
#define byte    DInput3Reg    // This parameter is represented from Note10
#define byte    DInput3Bit    // This parameter is represented from Note11
#define byte    DInput4LDN    // This parameter is represented from Note12
#define byte    DInput4Reg    // This parameter is represented from Note13
#define byte    DInput4Bit    // This parameter is represented from Note14
#define byte    DInput5LDN    // This parameter is represented from Note15
#define byte    DInput5Reg    // This parameter is represented from Note16
#define byte    DInput5Bit    // This parameter is represented from Note17
#define byte    DInput6LDN    // This parameter is represented from Note18
#define byte    DInput6Reg    // This parameter is represented from Note19
#define byte    DInput6Bit    // This parameter is represented from Note20
#define byte    DInput7LDN    // This parameter is represented from Note21
#define byte    DInput7Reg    // This parameter is represented from Note22
#define byte    DInput7Bit    // This parameter is represented from Note23
#define byte    DInput8LDN    // This parameter is represented from Note24
#define byte    DInput8Reg    // This parameter is represented from Note25
#define byte    DInput8Bit    // This parameter is represented from Note26
**********************************************************************************
```

```
*********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN   // This parameter is represented from Note27
#define byte   DOutput1Reg   // This parameter is represented from Note28
#define byte   DOutput1Bit   // This parameter is represented from Note29
#define byte   DOutput1Val   // This parameter is represented from Note30
#define byte   DOutput2LDN   // This parameter is represented from Note31
#define byte   DOutput2Reg   // This parameter is represented from Note32
#define byte   DOutput2Bit   // This parameter is represented from Note33
#define byte   DOutput2Val   // This parameter is represented from Note34
#define byte   DOutput3LDN   // This parameter is represented from Note35
#define byte   DOutput3Reg   // This parameter is represented from Note36
#define byte   DOutput3Bit   // This parameter is represented from Note37
#define byte   DOutput3Val   // This parameter is represented from Note38
#define byte   DOutput4LDN   // This parameter is represented from Note39
#define byte   DOutput4Reg   // This parameter is represented from Note40
#define byte   DOutput4Bit   // This parameter is represented from Note41
#define byte   DOutput4Val   // This parameter is represented from Note42
#define byte   DOutput5LDN   // This parameter is represented from Note43
#define byte   DOutput5Reg   // This parameter is represented from Note44
#define byte   DOutput5Bit   // This parameter is represented from Note45
#define byte   DOutput5Val   // This parameter is represented from Note46
#define byte   DOutput6LDN   // This parameter is represented from Note47
#define byte   DOutput6Reg   // This parameter is represented from Note48
#define byte   DOutput6Bit   // This parameter is represented from Note49
#define byte   DOutput6Val   // This parameter is represented from Note50
#define byte   DOutput7LDN   // This parameter is represented from Note51
#define byte   DOutput7Reg   // This parameter is represented from Note52
#define byte   DOutput7Bit   // This parameter is represented from Note53
#define byte   DOutput7Val   // This parameter is represented from Note54
#define byte   DOutput8LDN   // This parameter is represented from Note55
#define byte   DOutput8Reg   // This parameter is represented from Note56
#define byte   DOutput8Bit   // This parameter is represented from Note57
#define byte   DOutput8Val   // This parameter is represented from Note58
*********************************************************************************
```

```
**********************************************************************************
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DInput11LDN   // This parameter is represented from Note3-1
#define byte   DInput11Reg   // This parameter is represented from Note4-1
#define byte   DInput11Bit   // This parameter is represented from Note5-1
#define byte   DInput12LDN   // This parameter is represented from Note6-1
#define byte   DInput12Reg   // This parameter is represented from Note7-1
#define byte   DInput12Bit   // This parameter is represented from Note8-1
#define byte   DInput13LDN   // This parameter is represented from Note9-1
#define byte   DInput13Reg   // This parameter is represented from Note10-1
#define byte   DInput13Bit   // This parameter is represented from Note11-1
#define byte   DInput14LDN   // This parameter is represented from Note12-1
#define byte   DInput14Reg   // This parameter is represented from Note13-1
#define byte   DInput14Bit   // This parameter is represented from Note14-1
#define byte   DInput15LDN   // This parameter is represented from Note15-1
#define byte   DInput15Reg   // This parameter is represented from Note16-1
#define byte   DInput15Bit   // This parameter is represented from Note17-1
#define byte   DInput16LDN   // This parameter is represented from Note18-1
#define byte   DInput16Reg   // This parameter is represented from Note19-1
#define byte   DInput16Bit   // This parameter is represented from Note20-1
#define byte   DInput17LDN   // This parameter is represented from Note21-1
#define byte   DInput17Reg   // This parameter is represented from Note22-1
#define byte   DInput17Bit   // This parameter is represented from Note23-1
#define byte   DInput18LDN   // This parameter is represented from Note24-1
#define byte   DInput18Reg   // This parameter is represented from Note25-1
#define byte   DInput18Bit   // This parameter is represented from Note26-1
**********************************************************************************
```

```
**********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput11LDN   // This parameter is represented from Note27-1
#define byte   DOutput11Reg   // This parameter is represented from Note28-1
#define byte   DOutput11Bit   // This parameter is represented from Note29-1
#define byte   DOutput11Val   // This parameter is represented from Note30-1
#define byte   DOutput12LDN   // This parameter is represented from Note31-1
#define byte   DOutput12Reg   // This parameter is represented from Note32-1
#define byte   DOutput12Bit   // This parameter is represented from Note33-1
#define byte   DOutput12Val   // This parameter is represented from Note34-1
#define byte   DOutput13LDN   // This parameter is represented from Note35-1
#define byte   DOutput13Reg   // This parameter is represented from Note36-1
#define byte   DOutput13Bit   // This parameter is represented from Note37-1
#define byte   DOutput13Val   // This parameter is represented from Note38-1
#define byte   DOutput14LDN   // This parameter is represented from Note39-1
#define byte   DOutput14Reg   // This parameter is represented from Note40-1
#define byte   DOutput14Bit   // This parameter is represented from Note41-1
#define byte   DOutput14Val   // This parameter is represented from Note42-1
#define byte   DOutput15LDN   // This parameter is represented from Note43-1
#define byte   DOutput15Reg   // This parameter is represented from Note44-1
#define byte   DOutput15Bit   // This parameter is represented from Note45-1
#define byte   DOutput15Val   // This parameter is represented from Note46-1
#define byte   DOutput16LDN   // This parameter is represented from Note47-1
#define byte   DOutput16Reg   // This parameter is represented from Note48-1
#define byte   DOutput16Bit   // This parameter is represented from Note49-1
#define byte   DOutput16Val   // This parameter is represented from Note50-1
#define byte   DOutput17LDN   // This parameter is represented from Note51-1
#define byte   DOutput17Reg   // This parameter is represented from Note52-1
#define byte   DOutput17Bit   // This parameter is represented from Note53-1
#define byte   DOutput17Val   // This parameter is represented from Note54-1
#define byte   DOutput18LDN   // This parameter is represented from Note55-1
#define byte   DOutput18Reg   // This parameter is represented from Note56-1
#define byte   DOutput18Bit   // This parameter is represented from Note57-1
#define byte   DOutput18Val   // This parameter is represented from Note58-1
**********************************************************************************
```

```
*****************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //        Example, Read Digital I/O Pin 3 status
        // Output :
        //        InputStatus :
        //                0: Digital I/O Pin level is low
        //                1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

        // Procedure : AaeonSetOutputLevel
        // Input :
        //        Example, Set Digital I/O Pin 6 level
        AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit, DOutput6Val);
}
*****************************************************************************
```

```
*****************************************************************************
Boolean    AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
        Boolean PinStatus ;

        PinStatus = SIOBitRead(LDN, Register, BitNum);
        Return PinStatus ;
}
VOID    AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
        ConfigToOutputMode(LDN, Register, BitNum);
        SIOBitSet(LDN, Register, BitNum, Value);
}
*****************************************************************************
```

```
*****************************************************************************
VOID    SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID    SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID    SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID    SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID    SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

```
*****************************************************************************
Boolean    SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID    ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
        Byte TmpValue, OutputEnableReg;

        OutputEnableReg = Register-1;
        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, OutputEnableReg);
        TmpValue = IOReadByte(SIOData);
        TmpValue |= (1 << BitNum);
        IOWriteByte(SIOData, OutputEnableReg);
        SIOExitMBPnPMode();
}
*****************************************************************************
```