SPECIFICATION
FOR
LCM+CTP Module

MODULE No:	KD030NHFIN015B-C008A
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2024.05.24	V1.0	ALL	FIRST ISSUE

Contents

1.Basic Specifications

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorpho us silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Pan el, driver circuit,back-light unit. The resolution of a 3.0 " TFT-LCD contains 360x640 pixels, and can di splay up to 16.7M colors.

1.1 TFT Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area (AA)	36.72(H)*65.28(V) (3.0 inch)	mm	
Driver element	TFT active matrix	-	
Display colors	16.7M	colors	
Number of pixels	360(RGB)*640	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.102(H)*0.102(V)	mm	
Viewing angle	ALL	o'clock	
LCM Controller IC	ST7701S	-	
LCM Interface	2-Lane MIPI	-	
Display mode	Transmissive /Normally Black	-	
CTP And LCM Bonding Technology	Optical Bonding	-	
Operating temperature	-20～+70	℃	
Storage temperature	-30～+80	℃	

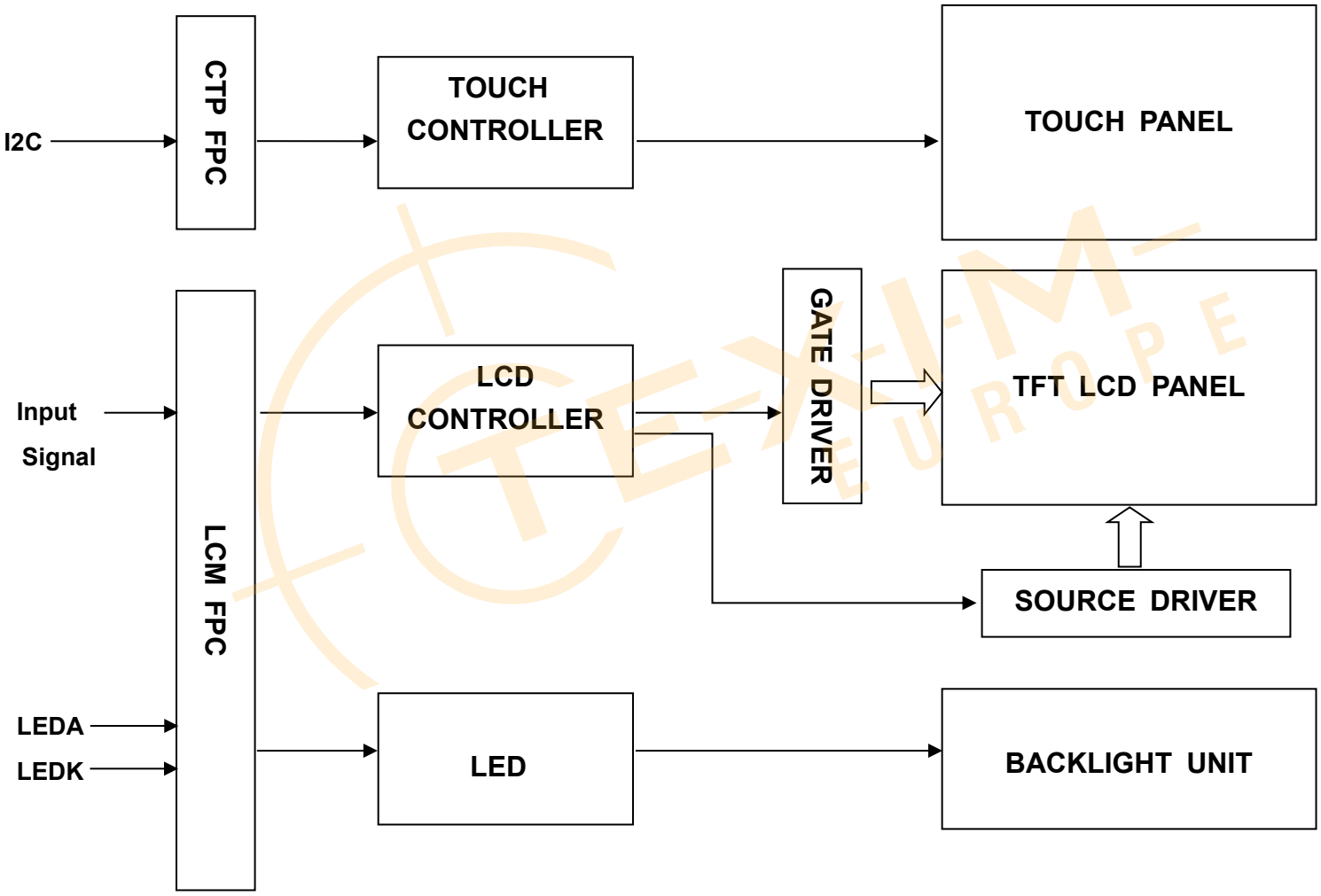
1.2 CTP Features

General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	360(H)*640(V)	-	
Structure	G+G	-	
Controller IC	FT5436	-	
Interface	I2C	-	
Slave Adress	0x38(7bit)/8bit:0x70(Write) 0x71(Read)	-	
Touch mode	Single point and Gestures	-	
	1.8 or 3.3		

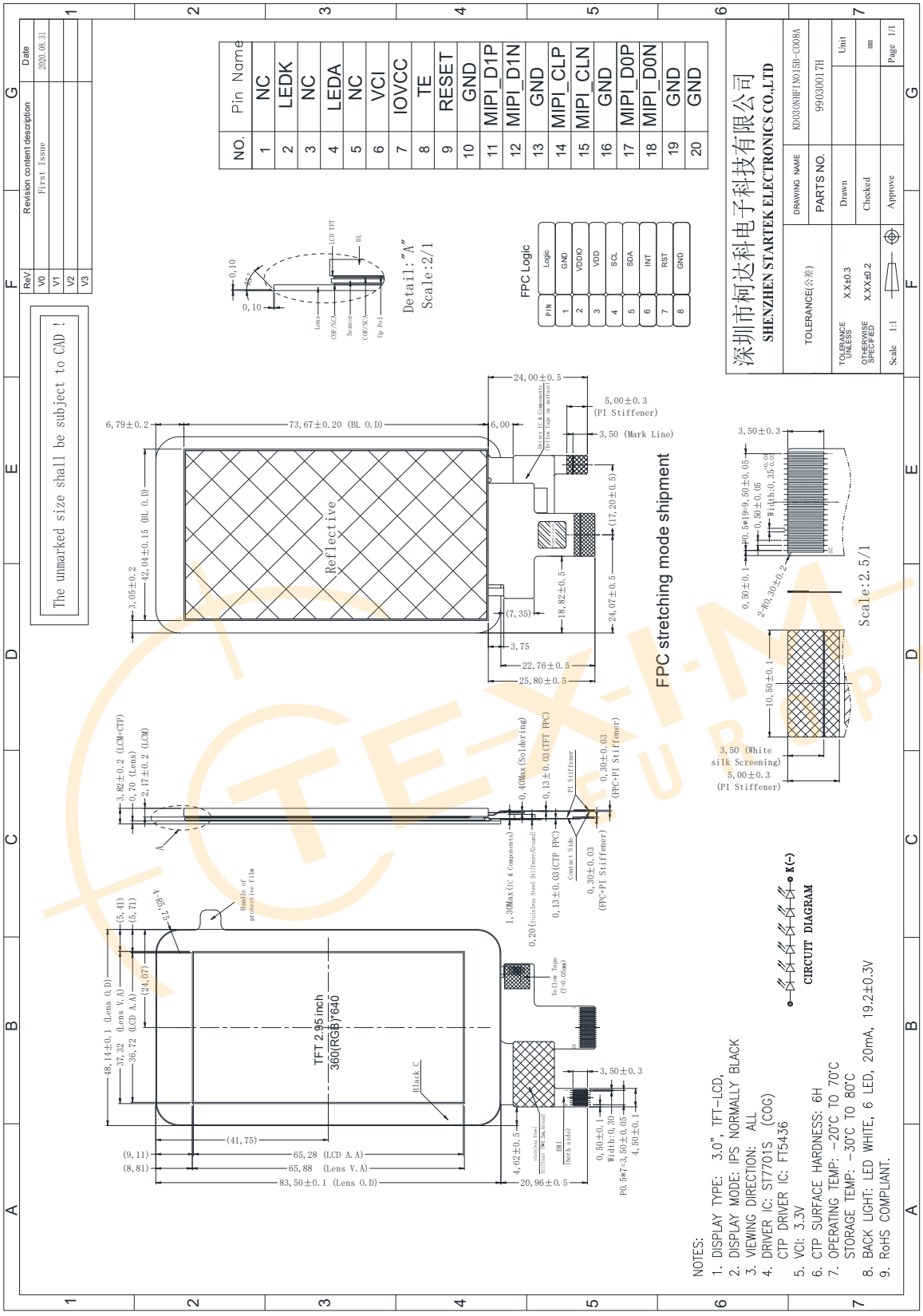
1.3 Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	48.14	-	mm	
	Vertical(V)	-	83.50	-	mm	
	Depth(D)	-	3.82	-	mm	
Weight		-	23	-	g	

2. Block Diagram



3. Outline dimension



4. Input terminal Pin Assignment

4.1 TFT PIN Definition

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	No connection	--
2	LEDK	Cathode pin of backlight	P
3	NC	No connection	--
4	LEDA	Anode pin of backlight	P
5	NC	No connection	--
6	VCI	Supply Voltage	P
7	IOVCC	Supply Voltage(I/O)	P
8	TE	For IC Test	O
9	RESET	The external reset input Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.	I
10	GND	Ground	P
11	MIPI_D1P	MIPI DSI differential data pair.	I/O
12	MIPI_D1N		
13	GND	Ground	P
14	MIPI_CLP	MIPI DSI differential clock pair.	I/O
15	MIPI_CLN		
16	GND	Ground	P
17	MIPI_D0P	MIPI DSI differential data pair.	I/O
18	MIPI_D0N		
19	GND	Ground	P
20	GND		

4.2 CTP PIN Definition

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	I/O power supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

5. LCD Optical Characteristics

5.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	600	800	--		
Response time	Rising	$T_{R+}T_F$		--	30	45	msec	
	Falling							
Color Gamut		S(%)		55	60.9	--	%	
Color Filter Chromaticity	White	W_X		0.2648	0.3048	0.3448		
		W_Y		0.2929	0.3329	0.3729		
	Red	R_X		0.5693	0.6093	0.6493		
		R_Y		0.3126	0.3526	0.3926		
	Green	G_X		0.2702	0.3102	0.3502		
		G_Y		0.5524	0.5924	0.6324		
	Blue	B_X		0.1082	0.1482	0.1882		
		B_Y		0.0377	0.0777	0.1177		
Viewing angle	Hor.	ΘL	CR>10	--	80	--		
		ΘR		--	80	--		
	Ver.	ΘU		--	80	--		
		ΘD		--	80	--		
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

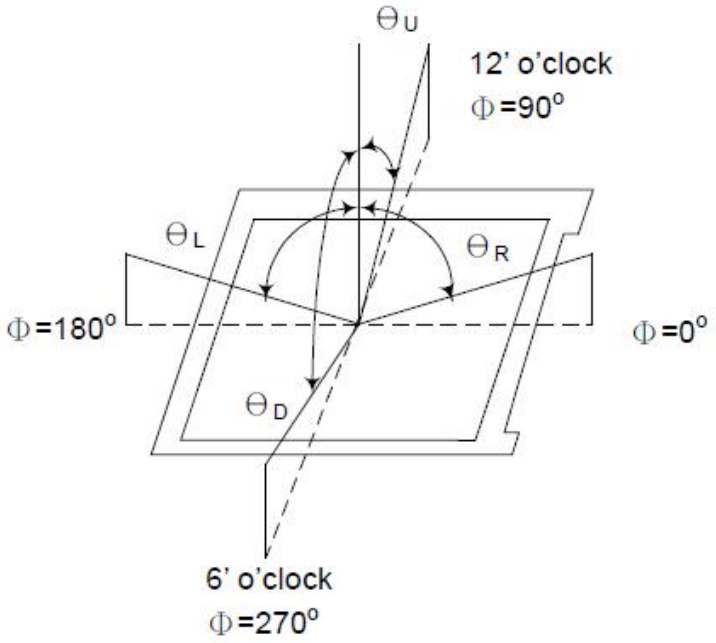
Ambient temperature : 25±2oC

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

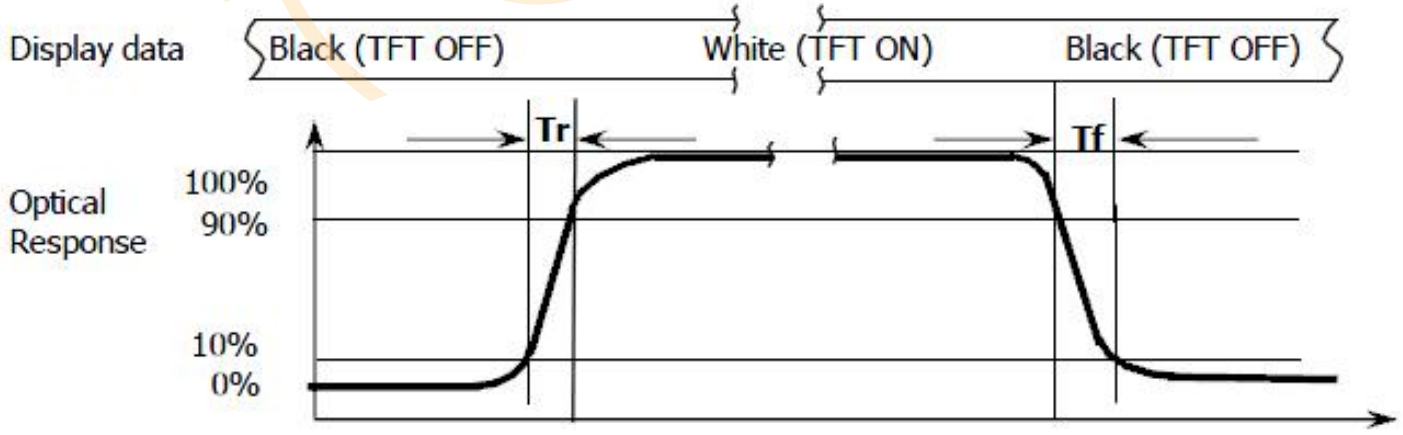
Note (1): Definition of Viewing Angle :



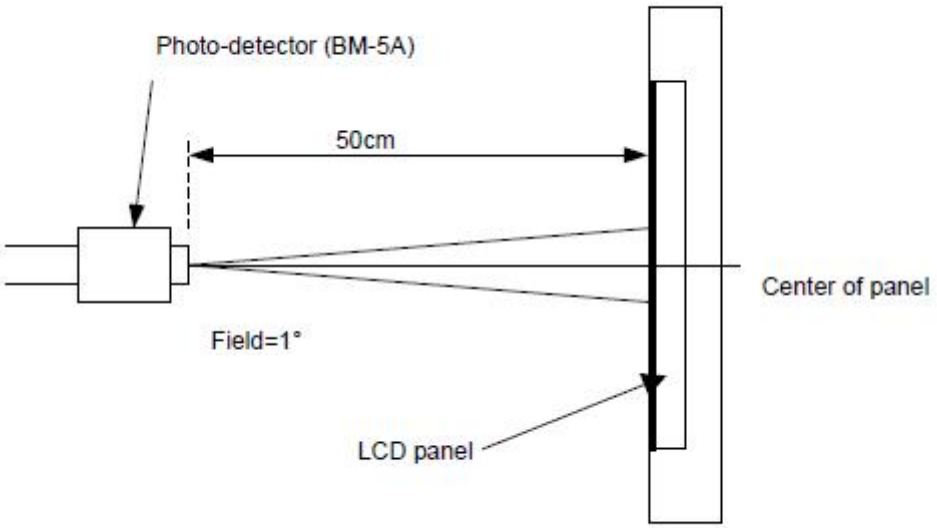
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



6. Electrical Characteristics

6.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCI	-0.3	4.8	V	Note1
Supply Voltage (Logic)	IOVCC	-0.3	4.6	V	
Operating temperature	T_{OP}	-20	+70	℃	
Storage temperature	T_{ST}	-30	+80	℃	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	3.6	V	
Supply Voltage (Logic)	IOVCC	1.65	1.8	3.3		
Normal mode Current	IDD	--	36	72	mA	
Level input voltage	V_{IH}	0.7*IOVCC	--	IOVCC	V	
	V_{IL}	GND	--	0.3*IOVCC	V	
Level output voltage	V_{OH}	0.8*IOVCC	--	IOVCC	V	
	V_{OL}	GND	--	0.2*IOVCC	V	

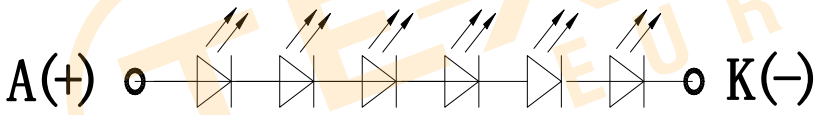
6.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 6 chips LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	20	--	mA	
Forward Voltage	V_F	16.8	--	20.4	V	
LCM Luminance	LV	250	300	--	cd/m2	Note3
LED life time	Hr	--	50000	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

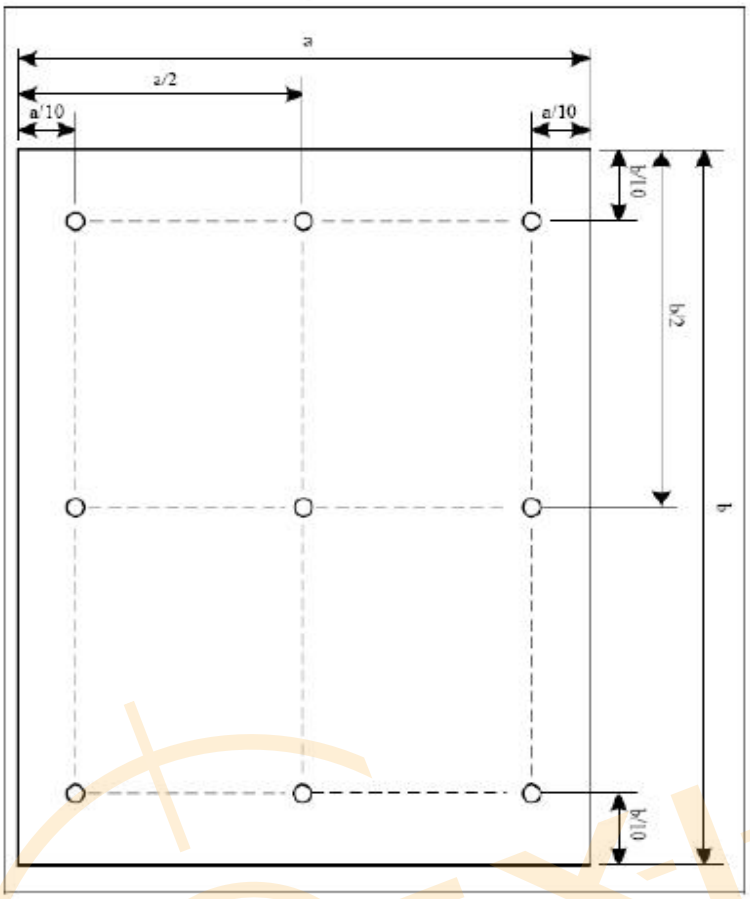
Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM

Note (3) Luminance Uniformity of these 9 points is defined as below:

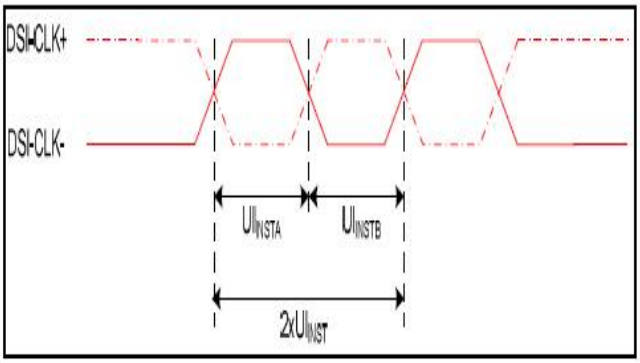


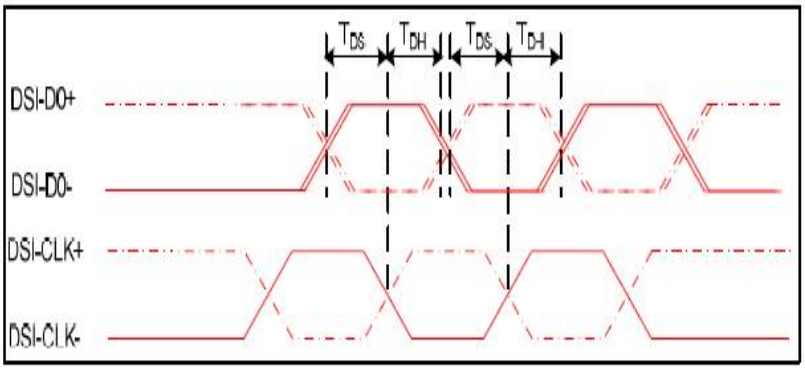
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

7. AC Characteristics

7.1 High Speed Mode





VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

7.2 Lowe Power Mode

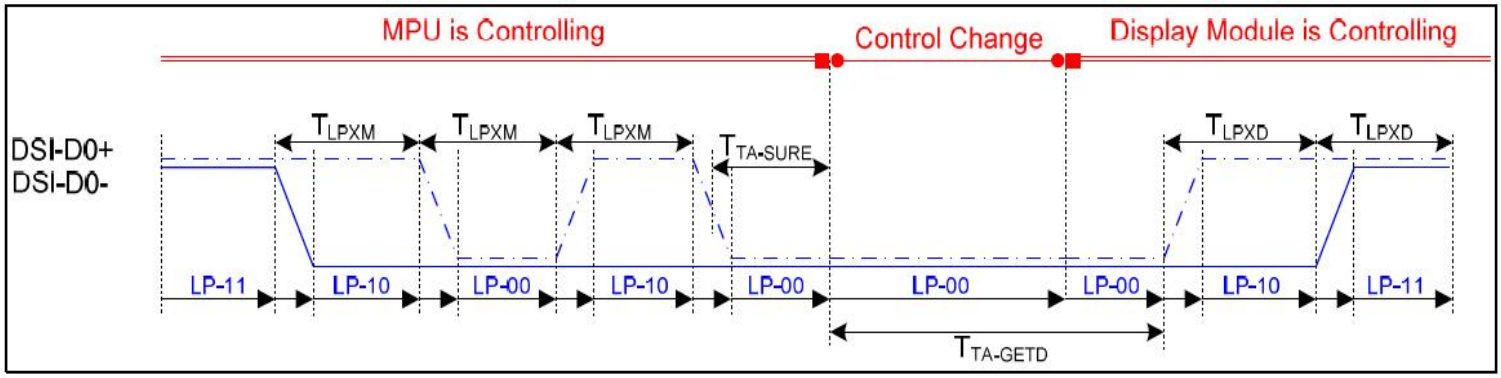
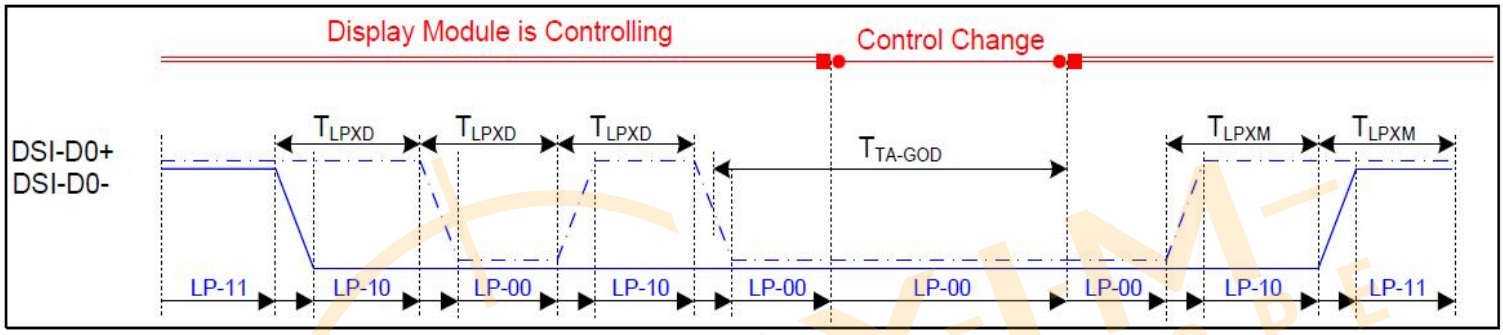


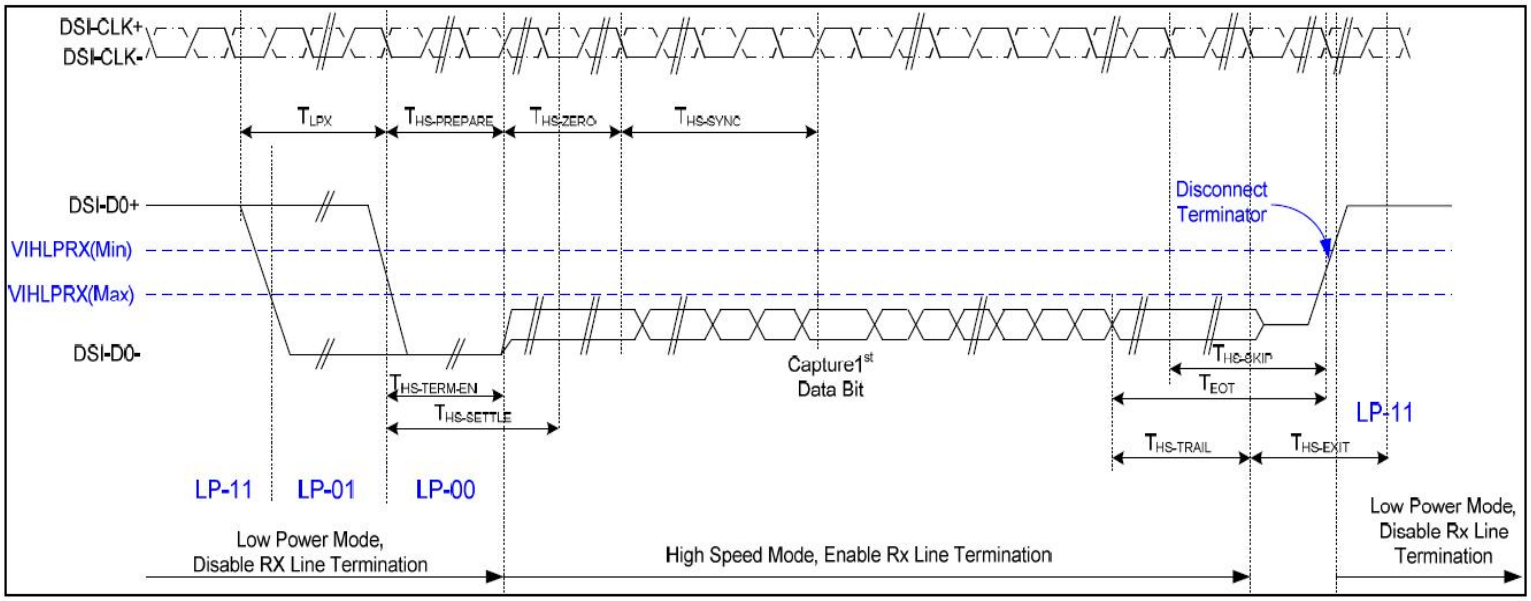
Figure 7 Bus Turnaround (BTA) from display module to MPU Timing

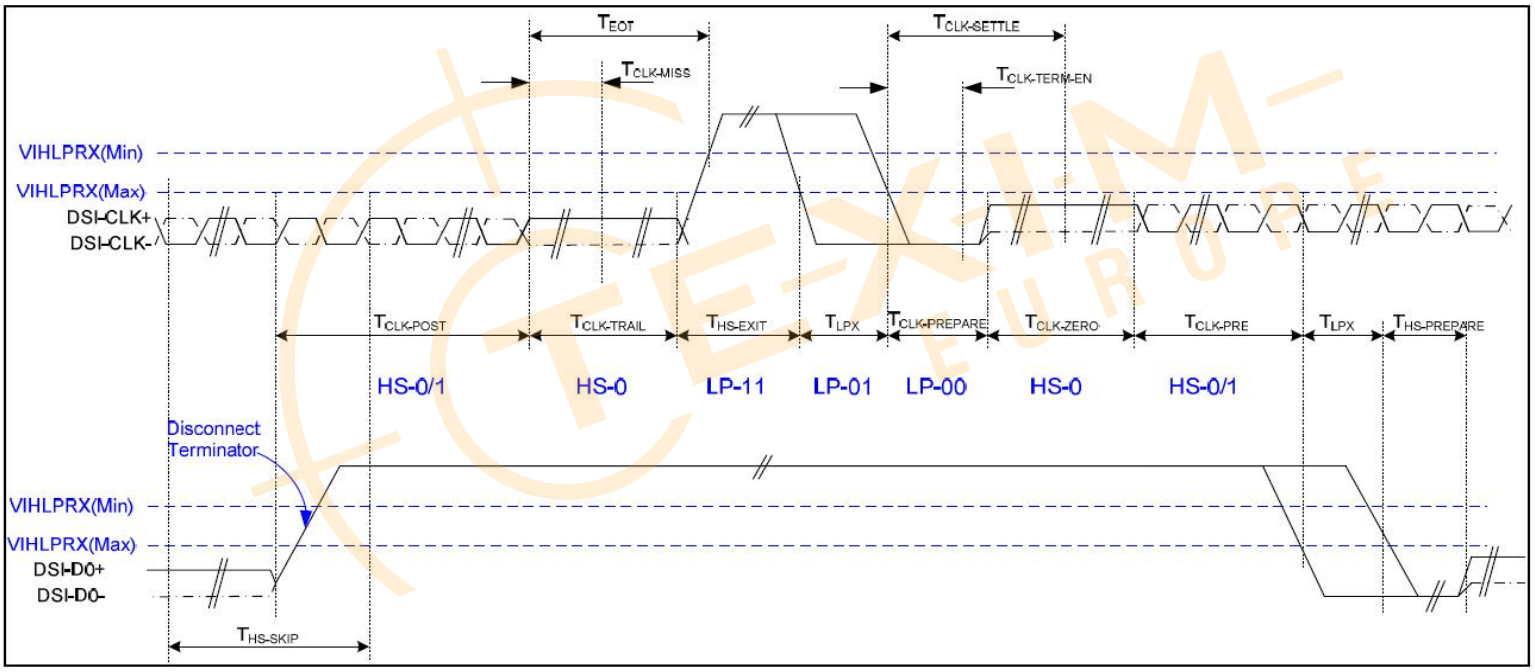


VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

7.3 DSI Bursts Mode





VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

7.4 Reset timing

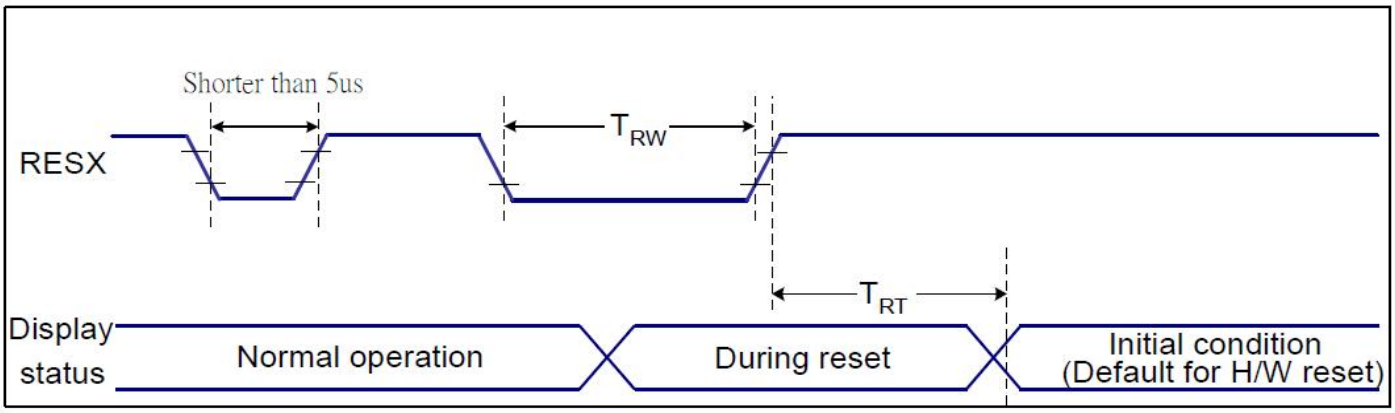


Figure 10 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Notes:

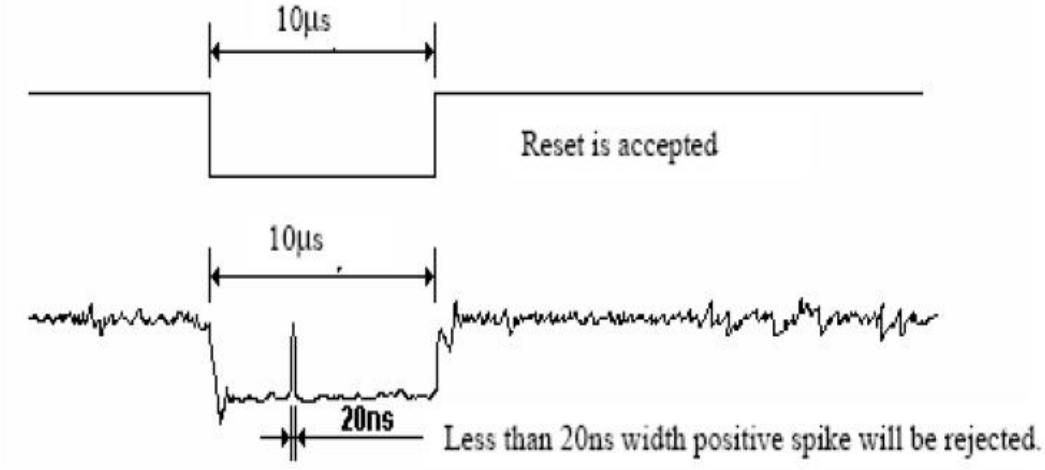
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. CTP Specification

8.1 Electrical Characteristics

8.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	1
I/O Digital Voltage	VDDIO	1.8	3.6	V	1
Operating temperature	T_{OP}	-20	+70	℃	-
Storage temperature	T_{ST}	-30	+80	℃	-

NOTES:

1. If used beyond the absolute maximum ratings, FT5436 may be permanently damaged. It is strongly recommanded that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

8.1.2 DC Electrical Characteristics (Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Digital supply voltage	VDD		2.8	3.3	3.6	V	
I/O Digital supply voltage	VDDIO		1.8	3.3	3.6	V	
Normal operation mode Current consumption	I_{opr}	VDD=2.8V Ta=25℃ MCLK= 17.5Mhz	-	11	-	mA	
Monitor mode Current consumption	I_{mon}		-	0.43	-	mA	
Sleep mode Current consumption	I_{slp}		-	42	-	uA	
Level input voltage	V_{IH}		$0.7V_{DDIO}$	-	V_{DDIO}	V	
	V_{IL}		-0.3	-	$0.3V_{DDIO}$	V	
Level output voltage	V_{OH}	I_{OH}=-0.1mA	$0.7V_{DDIO}$	-	-	V	
	V_{OL}	I_{OH}=0.1mA	-	-	$0.3V_{DDIO}$	V	

8.2 POWER ON/Reset/Wake Sequence

The GPIO such as INT and I2C are advised to be low before powering on. Reset should be pulled down to be low before powering on.INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Trst is more than 5ms.

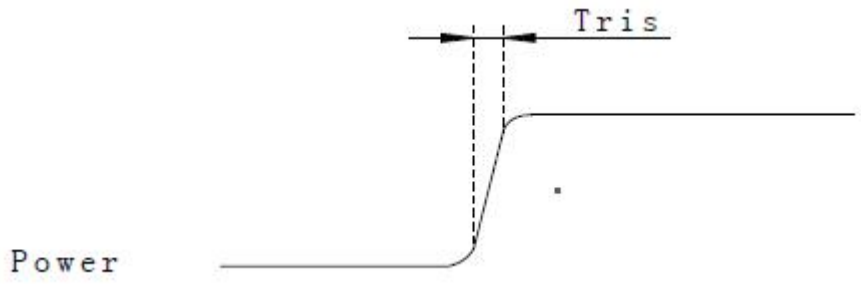


Figure 3-7 Power on time

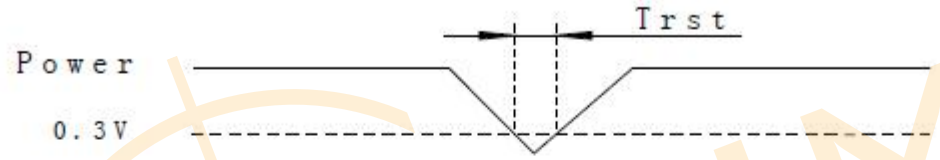


Figure 3-8 Power Cycle requirement

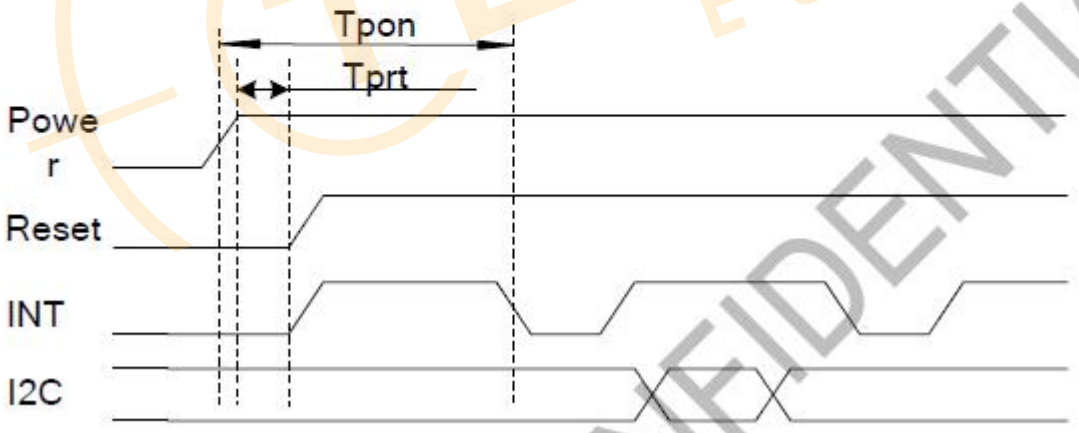


Figure 3-9 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on

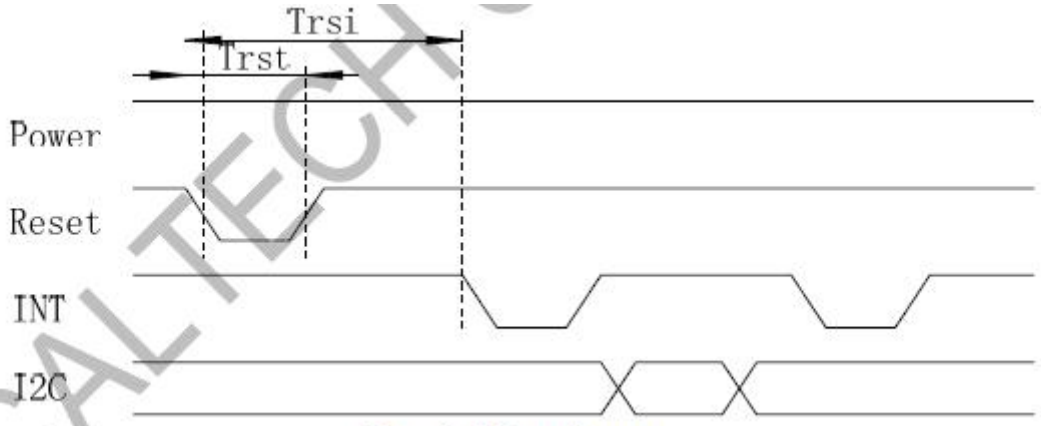


Figure 3-10 Reset Sequence

Table 3-5 Power on/Reset/Wake Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	-	3	ms
Tpon	Time of starting to report point after powering on	300	-	ms
Tprt	Time of being low after powering on	1	-	ms
Trsi	Time of starting to report point after resetting	300	-	ms
Trst	Reset time	5	-	ms

8.3 I2C Timing

FT5436 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4**.

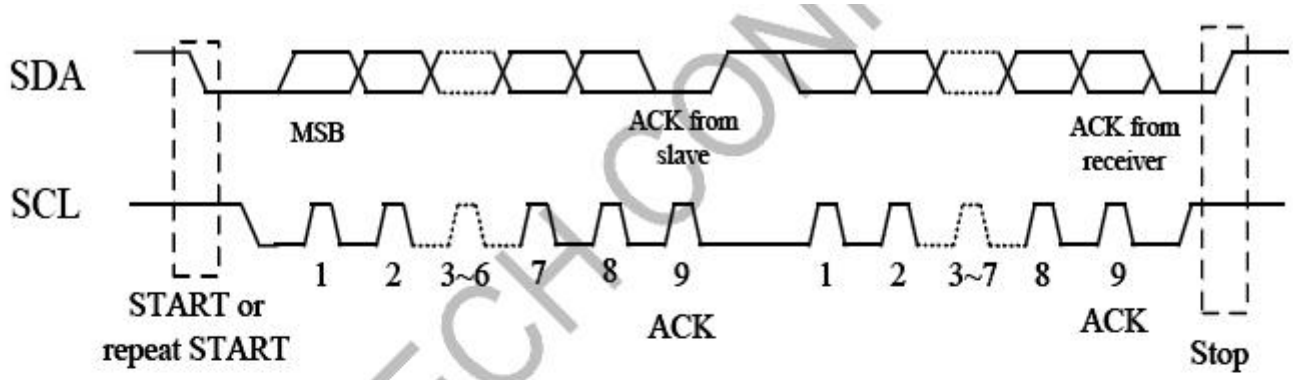


Figure 2-4 I2C Serial Data Transfer Format

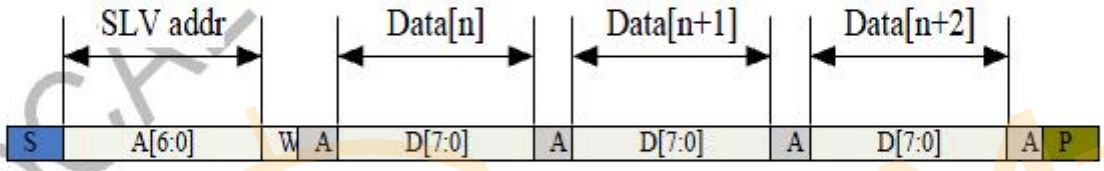


Figure 2-5 I2C master write, slave read

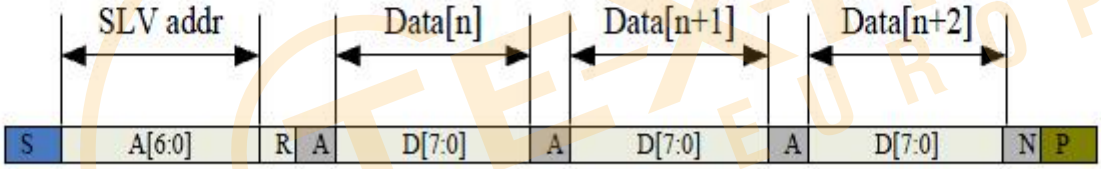


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

9. LCD Module Out-Going Quality Level

9.1 VISUAL & FUNCTION INSPECTION STANDARD

9.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

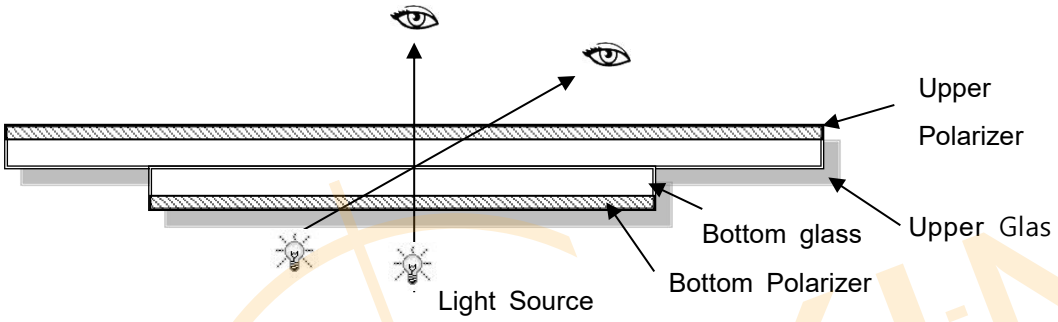
Temperature : 25±5℃

Humidity : 65%±10%RH

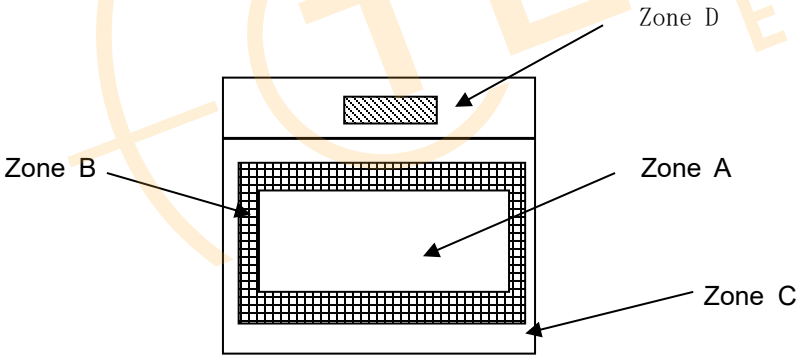
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



9.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

9.1.3 Sampling Plan

According to GB/T 2828-2012 ; , normal inspection, Class Ⅱ

AQL:

Major defect	Minor defect
0.65	1.5

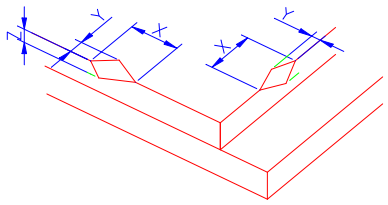
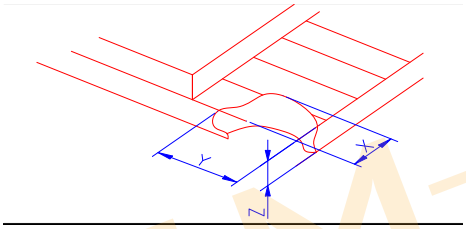
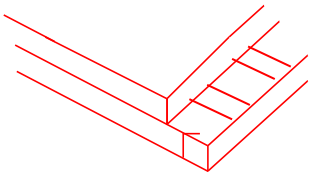
LCD: Liquid Crystal Display , LCM: Liquid Crystal Module, CTP: Capacitive Touch Panel

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc	Major
2	Missing	Missing components and etc	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed,deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer/CTP	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

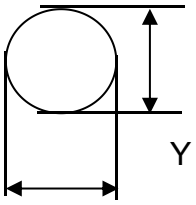
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

9.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

① light dot (black/white spot , pinhole, stain，etc.)

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

② Dim spot (light leakage、dent、dark spot，etc)

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance≧6mm)		
0.25<Φ≤0.4	2(distance≧6mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance≧6mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	3(distance≧6mm)		
Φ>0.4	0		

3.0 LCD Pixel defect

Pixel bad points

Item	Zone A	Acceptable Qt
Bright dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Dark dot	Random	N≤2
	2 dots adjacent	N≤0
	3 dots adjacent	N≤0
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm
Total bright and dark dot		N≤4

Note:

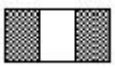
A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

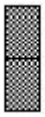
C) 2 dot adjacent = 1 pair = 2 dots

Picture:

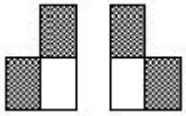
2 dot adjacent



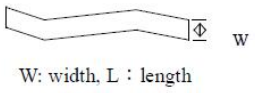
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)
 

N：Count</td>
<td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.04</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.04<W≤0.05</td><td>L≤2.0</td><td colspan="2">N≤1</td></tr>
<tr><td>W>0.05</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brightness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Waving/ Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
<tr>
<td>8.0</td>
<td>CTP Related</td>
<td>CTP Cover sensor accidented black/white spot</td>
<td>
<table>
<tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.1<Φ≤0.2</td><td colspan="2">3（distance≧6mm）</td></tr>
<tr><td>0.20<Φ≤0.25</td><td colspan="2">2（distance≧6mm）</td></tr>
<tr><td>Φ＞0.25</td><td colspan="2">0</td></tr>
</table>
</td>
</tr>
</table>

CTP Cover scratch

Width(mm)	Ignore (mm)	Acceptable Qty		
		A	B	C
Φ≤0.03	Ignore	Ignore		
0.03<W≤0.04	L≤3.0	N≤2		
0.04<W≤0.05	L≤2.0	N≤1		
0.05<W	Define as spot defect			

CTP Cover Pinhole/ Lack of ink

Zone / Size (mm)	Acceptable Qty
	C
Φ≤0.1	Ignore
0.1<Φ≤0.25	3(distance≧6mm)
0.25<Φ≤0.3	2(distance≧6mm)
Φ>0.3	0

CTP Bonding bubble/ accidented spot

Size Φ(mm)	Acceptable Qty	
	A	B
Φ≤0.1	Ignore	
0.1<Φ≤0.2	3(distance≧6mm)	
0.2<Φ≤0.25	2(distance≧6mm)	
Φ>0.25	0	

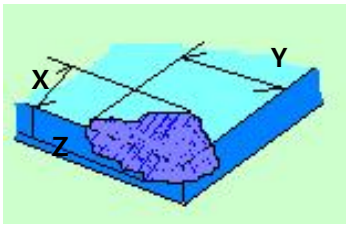
Assembly deflection

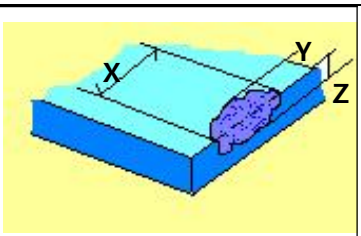
beyond the edge of backlight ≤0.2mm

CTP cover broken
X : length
Y : width
Z : height

X	Y	Z
X≤0.5mm	Y≤0.5mm	Z<cover thickness

*
Circuitry broken is not allowed.



		CTP cover broken X : length Y : width Z : height	X: X≤0.3mm; Y: Y≤0.3mm; Z: Z<cover thickness * Circuitry broken is not allowed.	

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	CTP no function	Not allowed

10. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10℃,30 min ↔ 60℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

6. The color fading mura of polarizing filter should not care.

11. Cautions and Handling Precautions

11.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

11.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

12. Packing

----TBD----------

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Please contact us if you have any questions about the contents of the datasheet.

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