TFT DISPLAY SPECIFICATION

WINSTAR Display Co.,Ltd.
華凌光電股份有限公司

Winstar Display Co., LTD
華凌光電股份有限公司
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SPECIFICATION

CUSTOMER : _____

MODULE NO.: WFN0360A2T0YAMNN000

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION:** **DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
			葉虹蘭
ISSUED DATE: 2025/06/30			

TFT Display Inspection Specification: https://www.winstar.com.tw/technology/download.html
Precaution in use of TFT module: https://www.winstar.com.tw/technology/download/declaration.html

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MODLE NO：

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2025/06/30		First issue

Contents

1.Module Classification Information

W	F	N	0360	A2	T	0Y	A	M	N	N	0	00
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬

①	Brand：WINSTAR DISPLAY CORPORATION
②	Display Type：F→TFT Type, J→Custom TFT
③	N: Normal　E：EFD　M：MIP
④	Display Size：3.6” TFT
⑤	Model serials no.

⑥ Backlight Type：

F：	CCFL, White	T：	LED, White
S：	LED, High Light White	Z：	Nichia LED, White
N：	With out Backlight	A：	Front Light

⑦ LCD Polarize Type/ Temperature range/ Gray Scale Inversion Direction

Operating Temperature	Normal temperature				Super Wide temperature					
LCD tape	TN		IPS	VA	TN				IPS	VA
View angle	6H	12H			6H	12H	O-Film	OD-Film		
Reflective	AA	-	-	AT	AN	-	-	-	AW	AV
Transflective	0B	0E	-	02	0M	0P	-	-	08	04
Transmissive	0C	0F	0A	0T	0N	0Q	0R	0S	0W	0V

Operating Temperature	Wide temperature									
LCD tape	TN								IPS	VA
View angle	6H	12H	2H	3H	9H	O-Film	OD-Film	All View		
Reflective	AG	AJ	AB	-	-	-	-	05	AY	AX
Transflective	0H	0K	-	0G	0D	0U	-	-	07	03
Transmissive	0I	0L	-	-	-	0Z	0J	-	0Y	0X

⑧

A：	TFT LCD	G：	TFT+ Screw holes
B：	TFT+ Screw holes+ Control board	H：	TFT+ D/V board
C：	TFT+ Screw holes + A/D board	I：	TFT+ Screw holes +D/V board
D：	TFT+ Screw holes + A/D board + Control board	J：	TFT+ Power board
E：	TFT+ Screw holes + Power board	Z：	TFT+ Power board (Embedded)
F：	TFT+ Control board		

⑨

A：Analog	B：6-bits parallel	D：Digital	E：eDP
L：LVDS	M：MIPI	S：SPI	

⑩ Interface:

A：8Bit	B：16Bit	E：eDP	H：HDMI	I：I2C Interface	M：MIPI
N：Without Control board	P：DP	R：RS232	S：SPI	U：USB	

⑪ TS:

A：	CTP + Optical bonding	B：	CTP + USB	C：	CTP
D：	CTP + USB + Optical bonding	E：	RTP + Optical bonding	F：	CG + Optical bonding
H：	CTP + Only G-sensor	J：	CTP + Only G-sensor + USB	L：	CTP+ Hover Touch
N：	Without TS	Q：	in-cell	R：	on-cell
T：	RTP	U：	CG	V：	in-cell + CG
W：	on-cell + CG				

⑫	Version:
⑬	Serial No.: Serial number (00~99)

2.Summary

This is a color active matrix a-Si LCD Q-Panel, using a-Si (amorphous silicon) TFTs (Thin Film Transistors) as an active switching devices. The module has a 3.6 inch diagonally measured active area with 280x712 resolutions (280 horizontal by 712 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors.

3.General Specifications

Item	Dimension	Unit
Size	3.6	inch
Dot Matrix	280 x RGB x 712 (TFT)	dots
Module dimension	38.2 x 101.48 x 4.03	mm
Active area	33.6 x 85.44	mm
Pixel pitch	0.12 X 0.12	mm
LCD type	TFT, Normally Black, Transmissive	
Viewing Angle	85/85/85/85	
TFT Interface	4-Lanes MIPI	
Backlight Type	LED ,Normally White	
TFT Driver IC	FL7703NI or Equivalent	
With /Without TP	Without TP	
Surface	Anti-Glare	

*Color tone slight changed by temperature and driving voltage.

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	℃
Storage Temperature	TST	-30	—	+80	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≦ 60℃, 90% RH MAX. Temp.＞60℃, Absolute humidity shall be less than 90% RH at 60℃

5.Electrical Characteristics

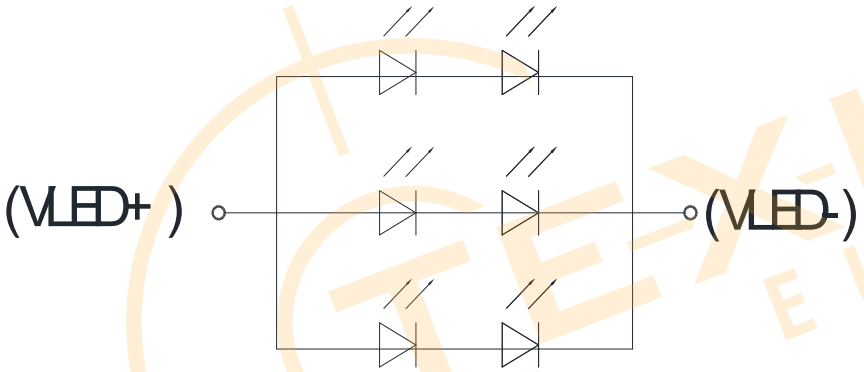
5.1. TFT LCD Module

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Analog Supply voltage	VCC	2.5	2.8	3.3	V	
Analog supply current	I_{CC}	-	65	98.0	mA	VCC=2.8V
Logic input voltage	VIH	0.7*VCC	-	VCC	V	
	VIL	GND	-	0.3*VCC	V	

5.2. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	-	-	90	-	mA	-
LED voltage	VLED+	5.5	6.0	6.8	V	Note 1
LED Life Time	-	50,000	-	-	Hr	Note 2,3,4

Note 1 : There are 1 Groups LED



Note 2 : Ta = 25 ℃

Note 3 : Brightness to be decreased to 50% of the initial value

Note 4 : The single LED lamp case

6.DC Characteristics

6.1. DSI DC Characteristics

LP Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps

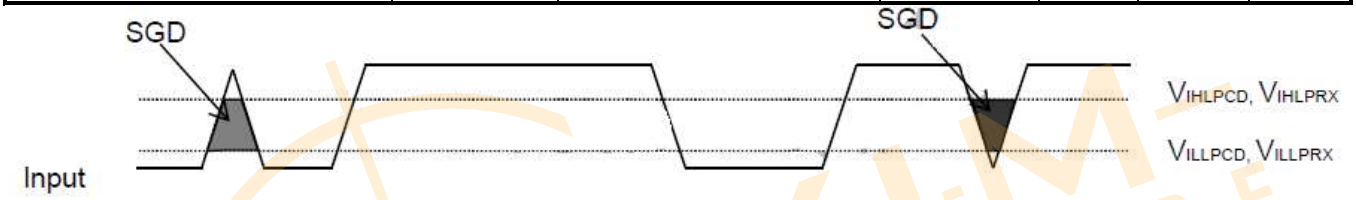


Figure 1: Input glitch rejections of low-power receivers

High Speed Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF

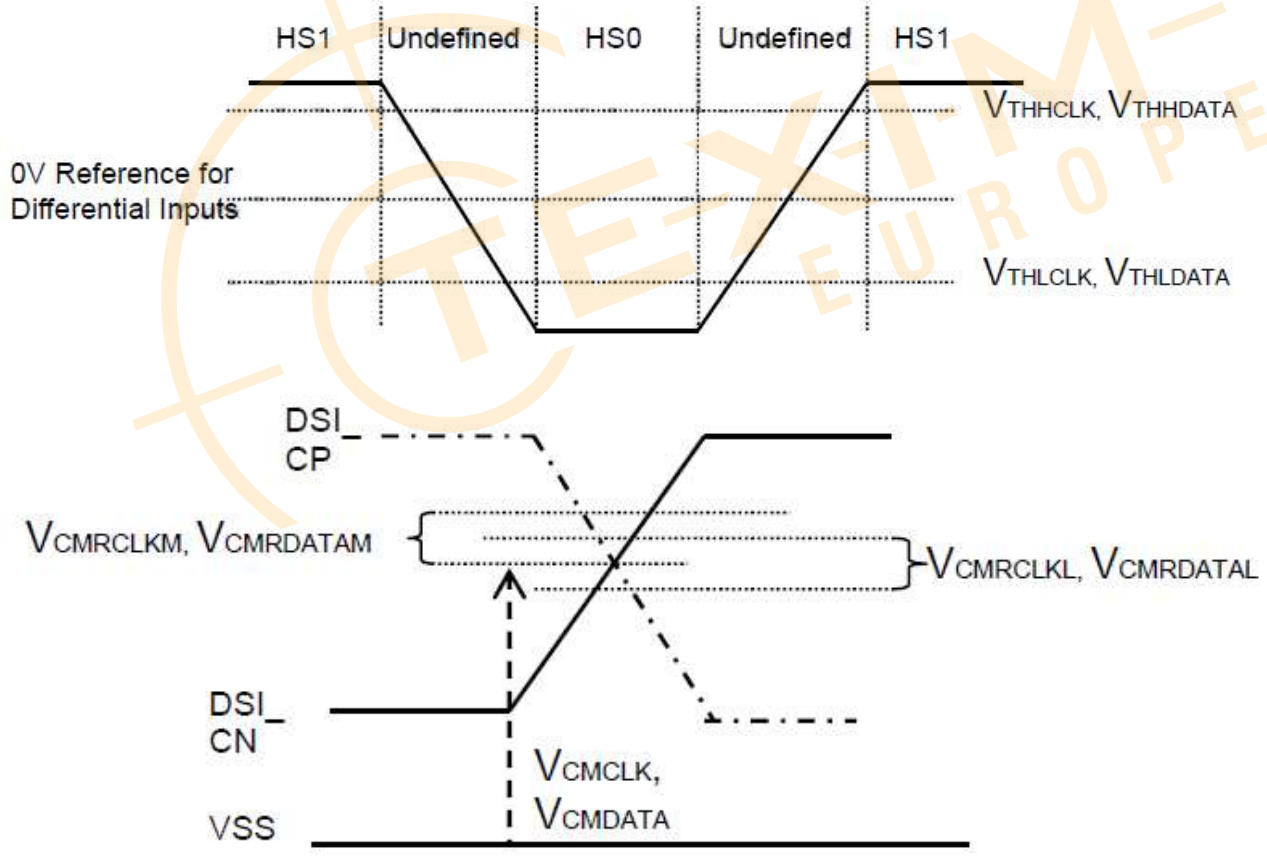


Figure 2: Differential voltage range and Command mode voltage

7.AC characteristics

7.1. DSI Interface Timing Characteristics

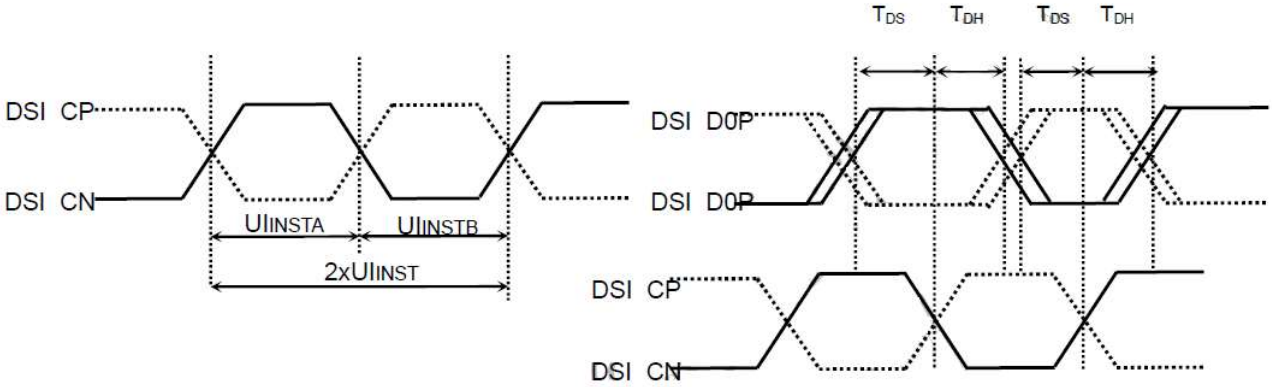


Figure 3: DSI clock timing Characteristics

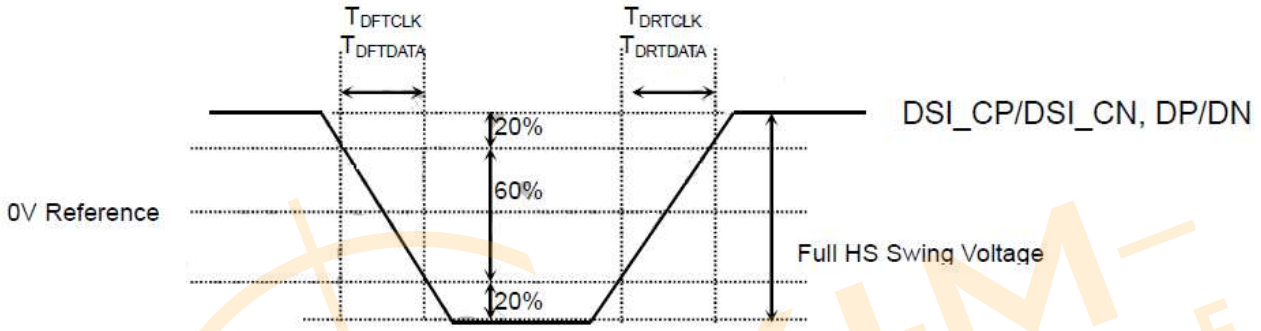


Figure 4: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V,TA = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	$2xU_{INST}$	4LANE：3.30 3LANE：2.85 @ VDDD=1.8V	-	25	ns
	UI instantaneous	U_{INSTA} U_{INSTB}	4LANE：1.67 3LANE：1.43 @ VDDD=1.8V	-	12.5	ns
DP/DN	Data to clock setup time	T_{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T_{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T_{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T_{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	$T_{DRTDATA}$	150	-	0.3UI	ps
	Differential fall time for data	$T_{DFTDATA}$	150	-	0.3UI	ps

Table 1: DSI High Speed Mode Characteristics

Low Power Mode

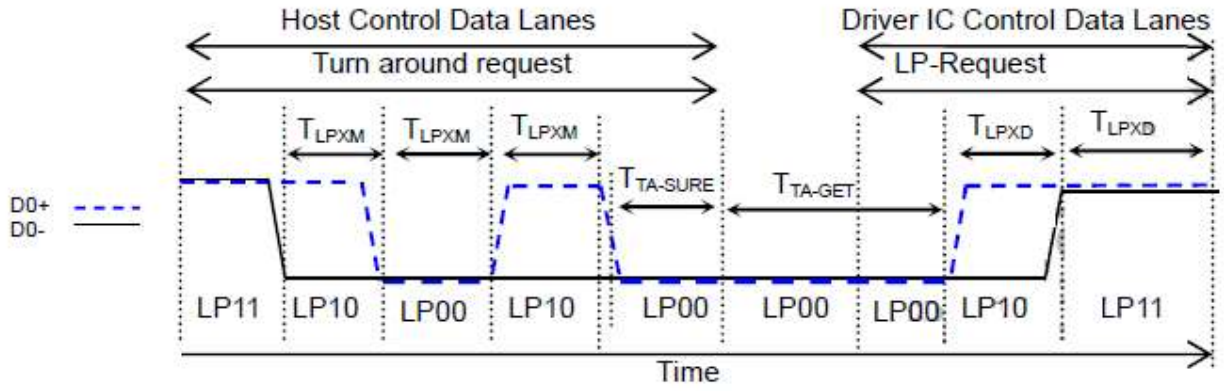


Figure 5: BTA from HOST to Display Module Timing

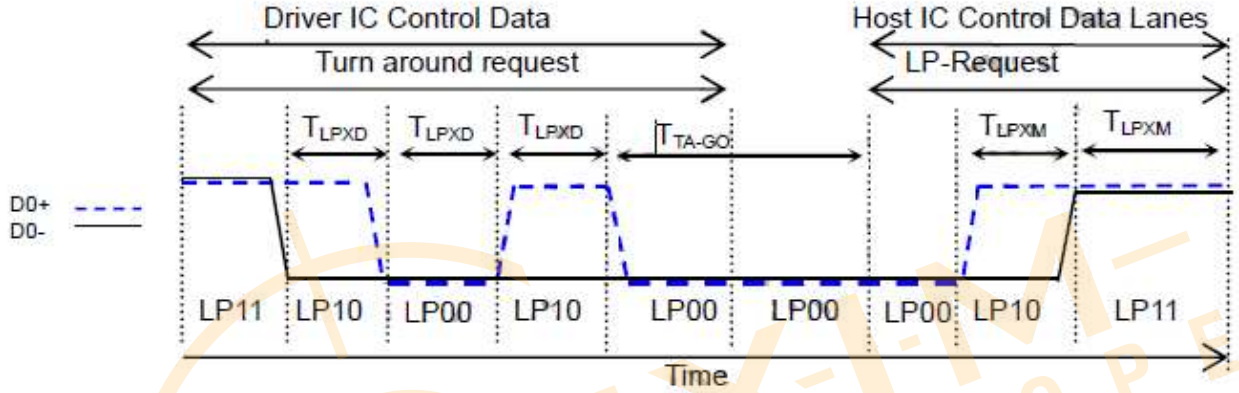


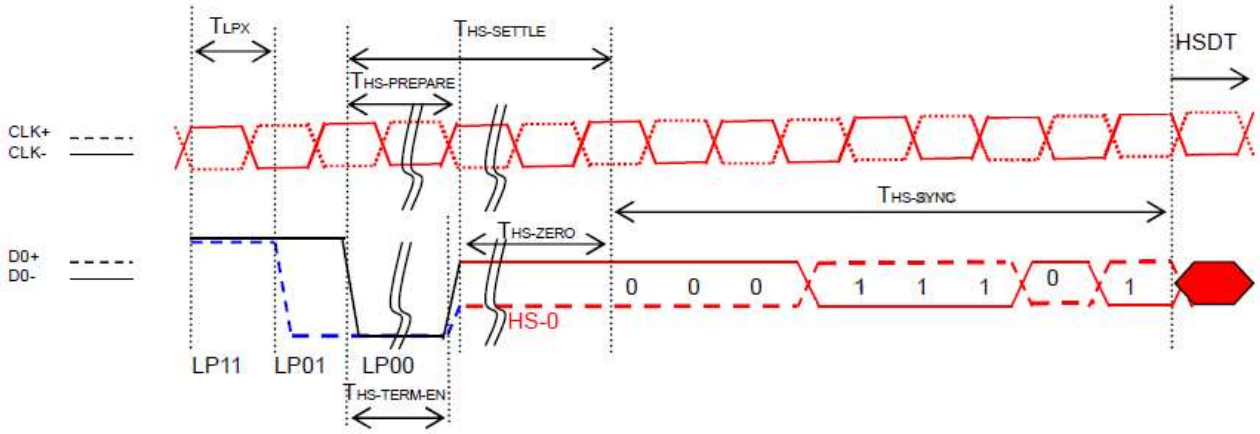
Figure 6: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,TA = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host → Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module → Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2xT_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5xT_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4xT_{LPXD}$	-	-	ns

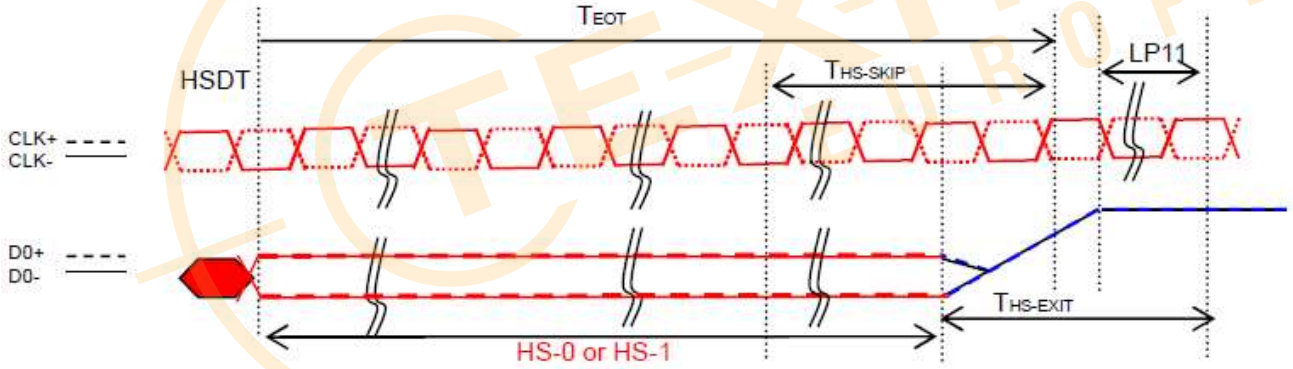
Table 2: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5xT_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4xT_{LPXD}$	-	-	ns

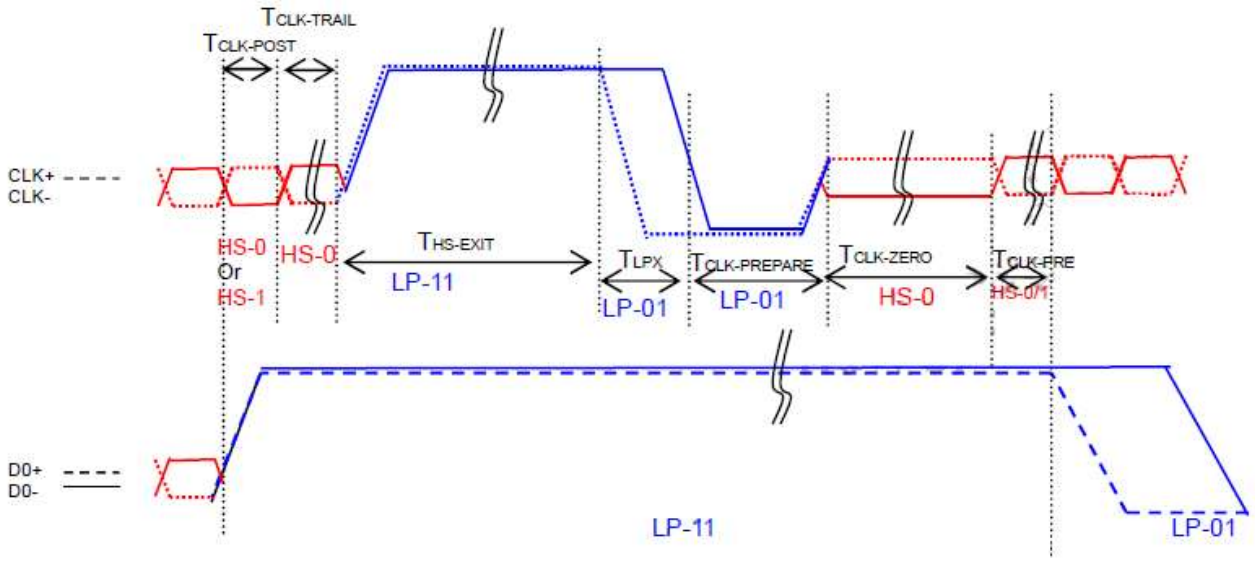
Table 3: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 4: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 5: Clock Lanes High Speed Mode to/from Low Power Mode Timing

7.2. Reset input timing

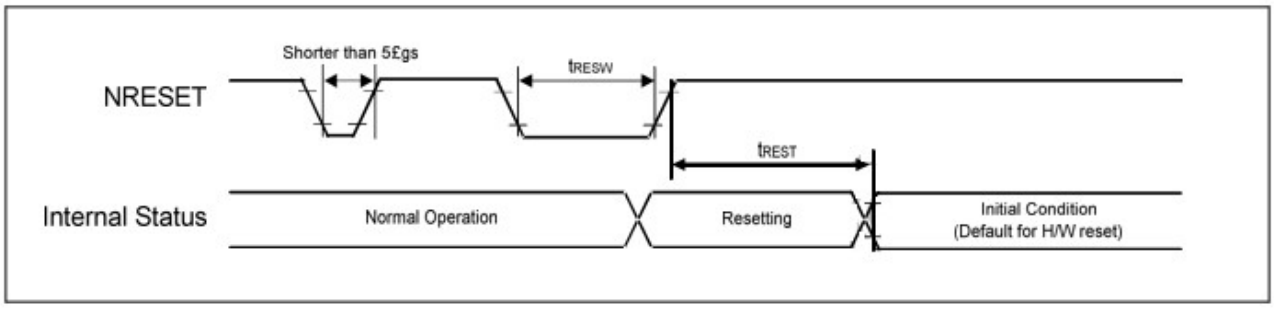


Figure 7: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 6: Reset Input Timing

Note:

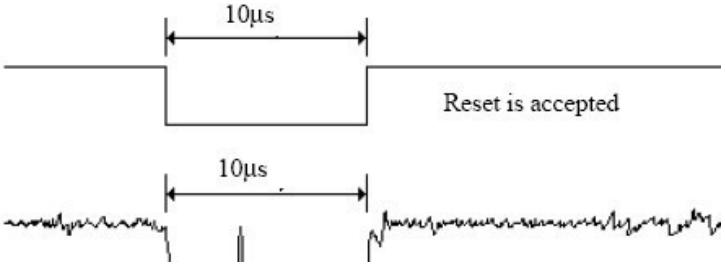
(1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3)During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

(4)Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.3. Timings Input timings for interface

Item	Symbol	Value			Unit
		Min.	Typ.	Max.	
HS low pulse width	HS	-	140	-	DCK
Horizontal back porch	HBP	-	200	-	DCK
Horizontal front porch	HFP	-	180	-	DCK
Horizontal blanking period	HBLK	-	NA	-	DCK
Horizontal active area	HDISP	-	280	-	DCK
Pixel Clock	PCLK	-	36	-	MHz
Vertical low pulse width	VS	-	4	-	Line
Vertical back porch	VBP	-	16	-	Line
Vertical front porch	VFP	-	16	-	Line
Vertical blanking period	VBK	-	NA	-	Line
Vertical active area	-	-	712	-	Line
Vertical Refresh rate	VRR	-	60.16	-	Hz

8.Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr+ Tf	θ=0°、Φ=0°	-	-	35	.ms	Note 3
Contrast ratio		CR	At optimized viewing angle	900	1200	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.251	0.301	0.351	-	Note 2,5,6
		Wy		0.279	0.329	0.379	-	
Viewing angle	Hor.	ΘR	CR≧10	80	85	-	Deg.	Note 1
		ΘL		80	85	-		
	Ver.	ΦT		80	85	-		
		ΦB		80	85	-		
Brightness		-	-	400	500	-	cd/m²	Center of display
Uniformity		(U)	-	75	-	-	%	Note 5

Ta=25±2℃,

Note 1: Definition of viewing angle range

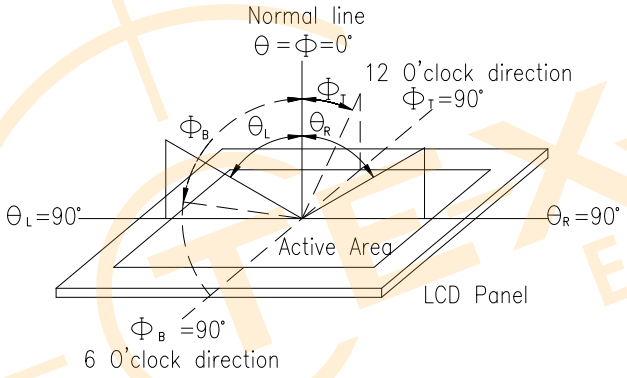


Fig. 8.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

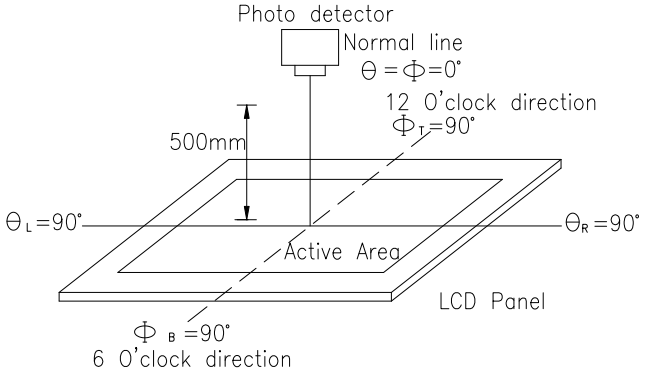
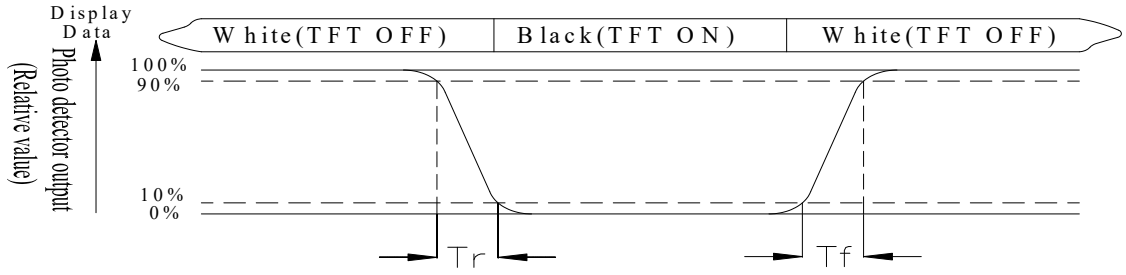


Fig. 8.2. Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.
Luminance Uniformity (U) = Lmin/Lmax x100%
L = Active area length
W = Active area width

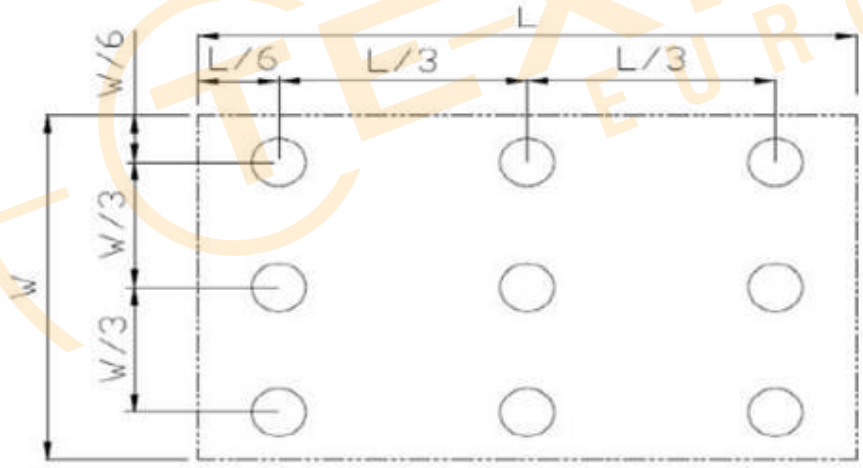


Fig8.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

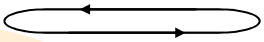
9.Interface

9.1. LCM PIN Definition

Pin No.	Symbol	Description
1	GND	Ground.
2	D3N	MIPI data input pins
3	D3P	
4	GND	Ground.
5	D2N	MIPI data input pins
6	D2P	
7	GND	Ground.
8	CLKN	MIPI clock input pins.
9	CLKP	
10	GND	Ground.
11	D1N	MIPI data input pins
12	D1P	
13	GND	Ground.
14	D0N	MIPI data input pins
15	D0P	
16	GND	Ground.
17	GND	Ground.
18	TE	Tearing effect output pin to synchronize to frame writing. If not used, open this pin
19	RESET	Reset signal pin
20	GND	Ground.
21-23	VCC	Power supply
24	GND	Ground.
25-26	NC	Not connect
27-28	VLED-	LED cathode
29-30	VLED+	LED anode

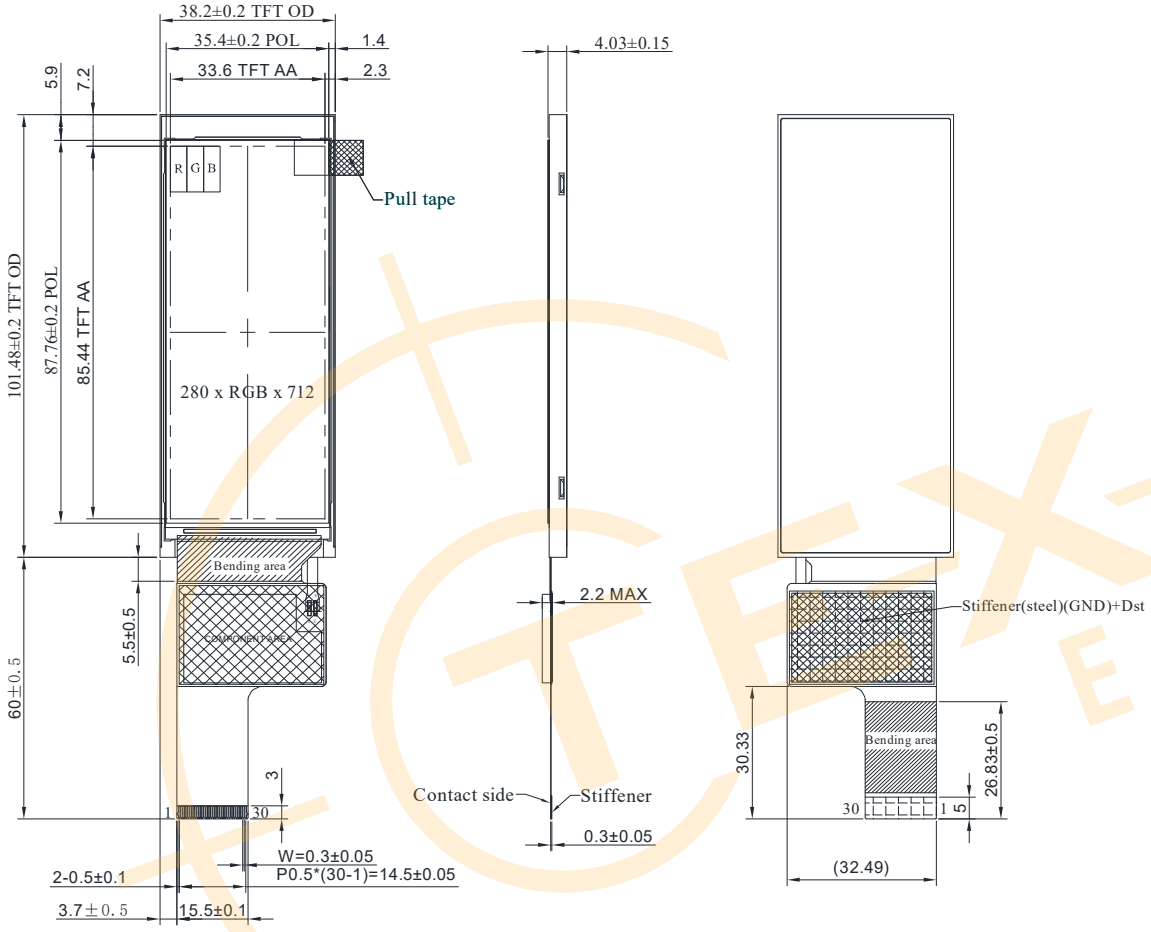
10.Reliability

Content of Reliability Test (Wide temperature, -20℃~70℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 240hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30℃ 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 240hrs	2
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 240hrs	1,2
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of storage -20℃ 25℃ 70℃  30min 5min 30min 1 cycle	-20℃/70℃ 10 cycles	2
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±TBD(contact), ±TBD(air), RS=330Ω CS=150pF 5 times	4

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.
Note3: The packing have to including into the vibration testing.
Note4: Endurance test applying the electric stress to the finished product housing

11.Contour Drawing



TFT FPC

PIN No.	SYMBOL	PIN No.	SYMBOL
1	GND	16	GND
2	D3N	17	GND
3	D3P	18	TE
4	GND	19	RESET
5	D2N	20	GND
6	D2P	21	VCC
7	GND	22	VCC
8	CLKN	23	VCC
9	CLKP	24	GND
10	GND	25	NC
11	D1N	26	NC
12	D1P	27	VLED-
13	GND	28	VLED-
14	D0N	29	VLED+
15	D0P	30	VLED+

The non-specified tolerance of dimension is ±0.3 mm .

12.Initial Code For Reference

```
void WFN0360A2_init(void)
{
    ssd2828_mipi_CMD_PA(0x04);
    ssd2828_mipi_write_data(0xB9);
    ssd2828_mipi_write_data(0xF1);
    ssd2828_mipi_write_data(0x12);
    ssd2828_mipi_write_data(0x87);

    ssd2828_mipi_CMD_PA(0x04);
    ssd2828_mipi_write_data(0xB2);
    ssd2828_mipi_write_data(0xB2);
    ssd2828_mipi_write_data(0x15);
    ssd2828_mipi_write_data(0x70);

    ssd2828_mipi_CMD_PA(0x0B);
    ssd2828_mipi_write_data(0xB3);
    ssd2828_mipi_write_data(0x10);
    ssd2828_mipi_write_data(0x10);
    ssd2828_mipi_write_data(0x28);
    ssd2828_mipi_write_data(0x28);
    ssd2828_mipi_write_data(0x03);
    ssd2828_mipi_write_data(0xFF);
    ssd2828_mipi_write_data(0x00);
    ssd2828_mipi_write_data(0x00);
    ssd2828_mipi_write_data(0x00);
    ssd2828_mipi_write_data(0x00);

    ssd2828_mipi_CMD_PA(0x02);
    ssd2828_mipi_write_data(0xB4);
    ssd2828_mipi_write_data(0x80);

    ssd2828_mipi_CMD_PA(0x03);
    ssd2828_mipi_write_data(0xB5);
    ssd2828_mipi_write_data(0x0D);
    ssd2828_mipi_write_data(0x0D);

    ssd2828_mipi_CMD_PA(0x03);
    ssd2828_mipi_write_data(0xB6);
    ssd2828_mipi_write_data(0x70);
    ssd2828_mipi_write_data(0x70);

    ssd2828_mipi_CMD_PA(0x05);
    ssd2828_mipi_write_data(0xB8);
    ssd2828_mipi_write_data(0x26);
    ssd2828_mipi_write_data(0x22);
    ssd2828_mipi_write_data(0xF0);
    ssd2828_mipi_write_data(0x13);
```

```
ssd2828_mipi_CMD_PA(0x1C);
ssd2828_mipi_write_data(0xBA);
ssd2828_mipi_write_data(0x33);
ssd2828_mipi_write_data(0x81);
ssd2828_mipi_write_data(0x05);
ssd2828_mipi_write_data(0xF9);
ssd2828_mipi_write_data(0x0E);
ssd2828_mipi_write_data(0x0E);
ssd2828_mipi_write_data(0x20);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x44);
ssd2828_mipi_write_data(0x25);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x91);
ssd2828_mipi_write_data(0x0A);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x01);
ssd2828_mipi_write_data(0x4F);
ssd2828_mipi_write_data(0x01);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x37);

ssd2828_mipi_CMD_PA(0x02);
ssd2828_mipi_write_data(0xBC);
ssd2828_mipi_write_data(0x47);

ssd2828_mipi_CMD_PA(0x06);
ssd2828_mipi_write_data(0xBF);
ssd2828_mipi_write_data(0x02);
ssd2828_mipi_write_data(0x10);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x80);
ssd2828_mipi_write_data(0x04);

ssd2828_mipi_CMD_PA(0x0A);
ssd2828_mipi_write_data(0xC0);
ssd2828_mipi_write_data(0x73);
ssd2828_mipi_write_data(0x73);
ssd2828_mipi_write_data(0x50);
ssd2828_mipi_write_data(0x50);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x12);
```

```
ssd2828_mipi_write_data(0x73);
ssd2828_mipi_write_data(0x00);

ssd2828_mipi_CMD_PA(0x12);
ssd2828_mipi_write_data(0xC1);
ssd2828_mipi_write_data(0x54);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x32);
ssd2828_mipi_write_data(0x32);
ssd2828_mipi_write_data(0x99);
ssd2828_mipi_write_data(0xE4);
ssd2828_mipi_write_data(0x77);
ssd2828_mipi_write_data(0x77);
ssd2828_mipi_write_data(0xCC);
ssd2828_mipi_write_data(0xCC);
ssd2828_mipi_write_data(0xFF);
ssd2828_mipi_write_data(0xFF);
ssd2828_mipi_write_data(0x11);
ssd2828_mipi_write_data(0x11);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x32);

ssd2828_mipi_CMD_PA(0x0D);
ssd2828_mipi_write_data(0xC7);
ssd2828_mipi_write_data(0x10);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x0A);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0xED);
ssd2828_mipi_write_data(0xC5);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0xA5);

ssd2828_mipi_CMD_PA(0x05);
ssd2828_mipi_write_data(0xC8);
ssd2828_mipi_write_data(0x10);
ssd2828_mipi_write_data(0x40);
ssd2828_mipi_write_data(0x1E);
ssd2828_mipi_write_data(0x03);

ssd2828_mipi_CMD_PA(0x02);
ssd2828_mipi_write_data(0xCC);
ssd2828_mipi_write_data(0x0F);

ssd2828_mipi_CMD_PA(0x23);
ssd2828_mipi_write_data(0xE0);
```

```
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x0B);
ssd2828_mipi_write_data(0x12);
ssd2828_mipi_write_data(0x29);
ssd2828_mipi_write_data(0x3C);
ssd2828_mipi_write_data(0x3F);
ssd2828_mipi_write_data(0x47);
ssd2828_mipi_write_data(0x3D);
ssd2828_mipi_write_data(0x06);
ssd2828_mipi_write_data(0x0C);
ssd2828_mipi_write_data(0x0D);
ssd2828_mipi_write_data(0x12);
ssd2828_mipi_write_data(0x13);
ssd2828_mipi_write_data(0x11);
ssd2828_mipi_write_data(0x13);
ssd2828_mipi_write_data(0x13);
ssd2828_mipi_write_data(0x1B);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x0B);
ssd2828_mipi_write_data(0x12);
ssd2828_mipi_write_data(0x29);
ssd2828_mipi_write_data(0x3C);
ssd2828_mipi_write_data(0x3F);
ssd2828_mipi_write_data(0x47);
ssd2828_mipi_write_data(0x3D);
ssd2828_mipi_write_data(0x06);
ssd2828_mipi_write_data(0x0C);
ssd2828_mipi_write_data(0x0D);
ssd2828_mipi_write_data(0x12);
ssd2828_mipi_write_data(0x13);
ssd2828_mipi_write_data(0x11);
ssd2828_mipi_write_data(0x13);
ssd2828_mipi_write_data(0x13);
ssd2828_mipi_write_data(0x1B);

ssd2828_mipi_CMD_PA(0x08);
ssd2828_mipi_write_data(0xE1);
ssd2828_mipi_write_data(0x11);
ssd2828_mipi_write_data(0x11);
ssd2828_mipi_write_data(0x91);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);

ssd2828_mipi_CMD_PA(0x0F);
ssd2828_mipi_write_data(0xE3);
ssd2828_mipi_write_data(0x07);
ssd2828_mipi_write_data(0x07);
ssd2828_mipi_write_data(0x0B);
ssd2828_mipi_write_data(0x0B);
```

```
ssd2828_mipi_write_data(0x0B);
ssd2828_mipi_write_data(0x0B);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0xFF);
ssd2828_mipi_write_data(0x04);
ssd2828_mipi_write_data(0xC0);
ssd2828_mipi_write_data(0x10);

ssd2828_mipi_CMD_PA(0x40);
ssd2828_mipi_write_data(0xE9);
ssd2828_mipi_write_data(0xC8);
ssd2828_mipi_write_data(0x10);
ssd2828_mipi_write_data(0x0A);
ssd2828_mipi_write_data(0x10);
ssd2828_mipi_write_data(0x0E);
ssd2828_mipi_write_data(0x80);
ssd2828_mipi_write_data(0x38);
ssd2828_mipi_write_data(0x12);
ssd2828_mipi_write_data(0x31);
ssd2828_mipi_write_data(0x23);
ssd2828_mipi_write_data(0x4F);
ssd2828_mipi_write_data(0x86);
ssd2828_mipi_write_data(0x80);
ssd2828_mipi_write_data(0x38);
ssd2828_mipi_write_data(0x47);
ssd2828_mipi_write_data(0x08);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x4F);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x04);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x4F);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x04);
ssd2828_mipi_write_data(0x94);
ssd2828_mipi_write_data(0xA3);
ssd2828_mipi_write_data(0xF8);
ssd2828_mipi_write_data(0x18);
ssd2828_mipi_write_data(0x13);
ssd2828_mipi_write_data(0x57);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
```

```
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x94);
ssd2828_mipi_write_data(0xA2);
ssd2828_mipi_write_data(0xF8);
ssd2828_mipi_write_data(0x08);
ssd2828_mipi_write_data(0x02);
ssd2828_mipi_write_data(0x46);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x01);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x80);
ssd2828_mipi_write_data(0x38);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);

ssd2828_mipi_CMD_PA(0x3E);
ssd2828_mipi_write_data(0xEA);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x1A);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x01);
ssd2828_mipi_write_data(0x0A);
ssd2828_mipi_write_data(0x41);
ssd2828_mipi_write_data(0x01);
ssd2828_mipi_write_data(0x02);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x94);
ssd2828_mipi_write_data(0xA0);
ssd2828_mipi_write_data(0x8F);
ssd2828_mipi_write_data(0x28);
ssd2828_mipi_write_data(0x64);
ssd2828_mipi_write_data(0x20);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
```

```
ssd2828_mipi_write_data(0x94);
ssd2828_mipi_write_data(0xA1);
ssd2828_mipi_write_data(0x8F);
ssd2828_mipi_write_data(0x38);
ssd2828_mipi_write_data(0x75);
ssd2828_mipi_write_data(0x31);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x88);
ssd2828_mipi_write_data(0x23);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x01);
ssd2828_mipi_write_data(0xF0);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x02);
ssd2828_mipi_write_data(0xCB);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x00);
ssd2828_mipi_write_data(0x40);
ssd2828_mipi_write_data(0x80);
ssd2828_mipi_write_data(0x38);
ssd2828_mipi_write_data(0x40);
ssd2828_mipi_write_data(0x80);
ssd2828_mipi_write_data(0x38);
ssd2828_mipi_write_data(0x00);

ssd2828_mipi_CMD_PA(0x04);
ssd2828_mipi_write_data(0xEF);
ssd2828_mipi_write_data(0xFF);
ssd2828_mipi_write_data(0xFF);
ssd2828_mipi_write_data(0x01);

ssd2828_mipi_CMD_PA(0x01);
ssd2828_mipi_write_data(0x11);
delay_ms(250);

ssd2828_mipi_CMD_PA(0x01);
ssd2828_mipi_write_data(0x29);
```

```
        delay_ms(50);
}
```

winstar

LCM Sample Estimate Feedback Sheet

Module Number： _____ **Page: 1**

1、Panel Specification：

1.	Panel Type：	□ Pass	□ NG , _____
2.	View Direction：	□ Pass	□ NG , _____
3.	Numbers of Dots：	□ Pass	□ NG , _____
4.	View Area：	□ Pass	□ NG , _____
5.	Active Area：	□ Pass	□ NG , _____
6.	Operating Temperature：	□ Pass	□ NG , _____
7.	Storage Temperature：	□ Pass	□ NG , _____
8.	Others： _____		

2、Mechanical

1.	PCB Size：	□ Pass	□ NG , _____
2.	Frame Size：	□ Pass	□ NG , _____
3.	Material of Frame：	□ Pass	□ NG , _____
4.	Connector Position：	□ Pass	□ NG , _____
5.	Fix Hole Position：	□ Pass	□ NG , _____
6.	Backlight Position：	□ Pass	□ NG , _____
7.	Thickness of PCB：	□ Pass	□ NG , _____
8.	Height of Frame to PCB：	□ Pass	□ NG , _____
9.	Height of Module：	□ Pass	□ NG , _____
10.	Others：	□ Pass	□ NG , _____

3、Relative Hole Size：

1.	Pitch of Connector：	□ Pass	□ NG , _____
2.	Hole size of Connector：	□ Pass	□ NG , _____
3.	Mounting Hole size：	□ Pass	□ NG , _____
4.	Mounting Hole Type：	□ Pass	□ NG , _____
5.	Others：	□ Pass	□ NG , _____

4、Backlight Specification：

1.	B/L Type：	□ Pass	□ NG , _____
2.	B/L Color：	□ Pass	□ NG , _____
3.	B/L Driving Voltage (Reference for LED Type)：	□ Pass	□ NG , _____
4.	B/L Driving Current：	□ Pass	□ NG , _____
5.	Brightness of B/L：	□ Pass	□ NG , _____
6.	B/L Solder Method：	□ Pass	□ NG , _____
7.	Others：	□ Pass	□ NG , _____

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5、Electronic Characteristics of Module：

1.	Input Voltage：	□ Pass	□ NG ,_____
2.	Supply Current：	□ Pass	□ NG ,_____
3.	Driving Voltage for LCD：	□ Pass	□ NG ,_____
4.	Contrast for LCD：	□ Pass	□ NG ,_____
5.	B/L Driving Method：	□ Pass	□ NG ,_____
6.	Negative Voltage Output：	□ Pass	□ NG ,_____
7.	Interface Function：	□ Pass	□ NG ,_____
8.	LCD Uniformity：	□ Pass	□ NG ,_____
9.	ESD test：	□ Pass	□ NG ,_____
10.	Others：	□ Pass	□ NG ,_____

6、Summary：

Sales signature：_____
Customer Signature：_____ **Date：** ____/____/____

Disclaimer

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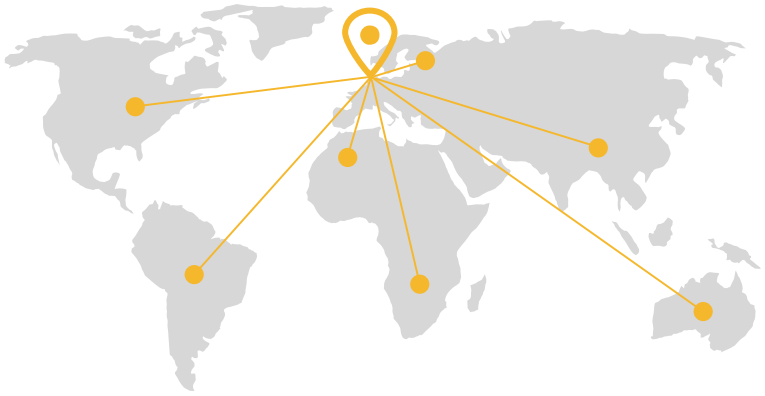

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