



SPECIFICATION FOR LCM Module

MODULE No:	KD050FWFIA019-01
CUSTOMER:	

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常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	



SHENZHEN STARTEK ELECTRONIC TECHNOLOGY CO., LTD

Revision History

KD050FWFIA019-01

REV

v1.0

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Stock For Sale

长期供货
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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 5.0''TFT-LCD contains 480x 854 pixels, and can display up to 65K/262K/16.7M colors.

* Features

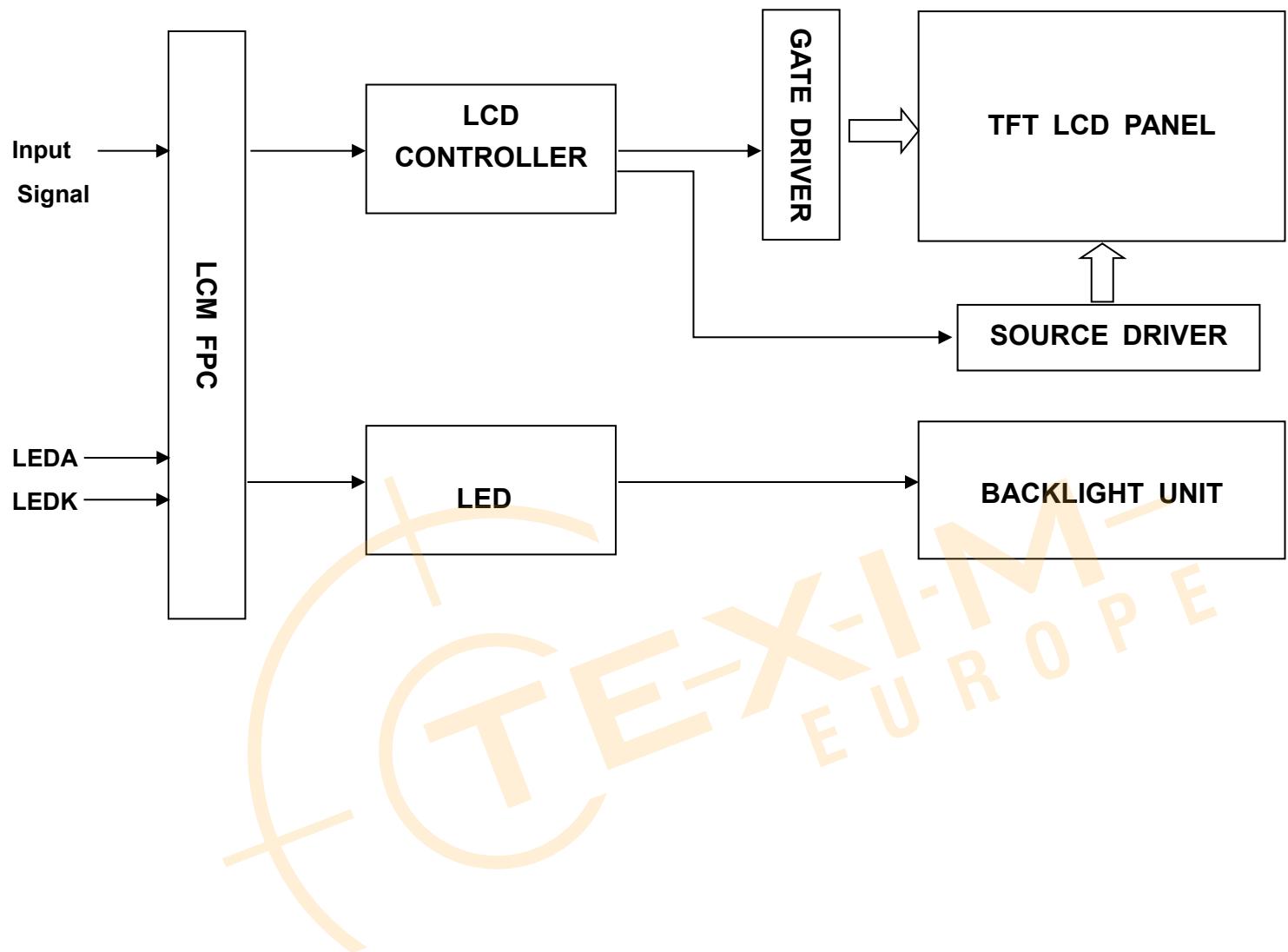
General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	61.632(H)*109.6536(V) (5.0inch)	mm	
Driver element	TFT active matrix	-	
Display colors	65/262K/16.7M	colors	
Number of pixels	480(RGB)*854	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.1284(H)*0.1284(V)	mm	
Viewing angle	ALL	o'clock	
Controller IC	ILI9806E	-	
LCM Interface	2-Lane MIPI	-	
Display mode	Transmissive /Normally Black	-	
Operating temperature	-20~+70	°C	
Storage temperature	-30~+80	°C	

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		67.06		mm	-
	Vertical(V)		121.85		mm	-
	Depth(D)		2.50		mm	-
Weight			TBD		g	-



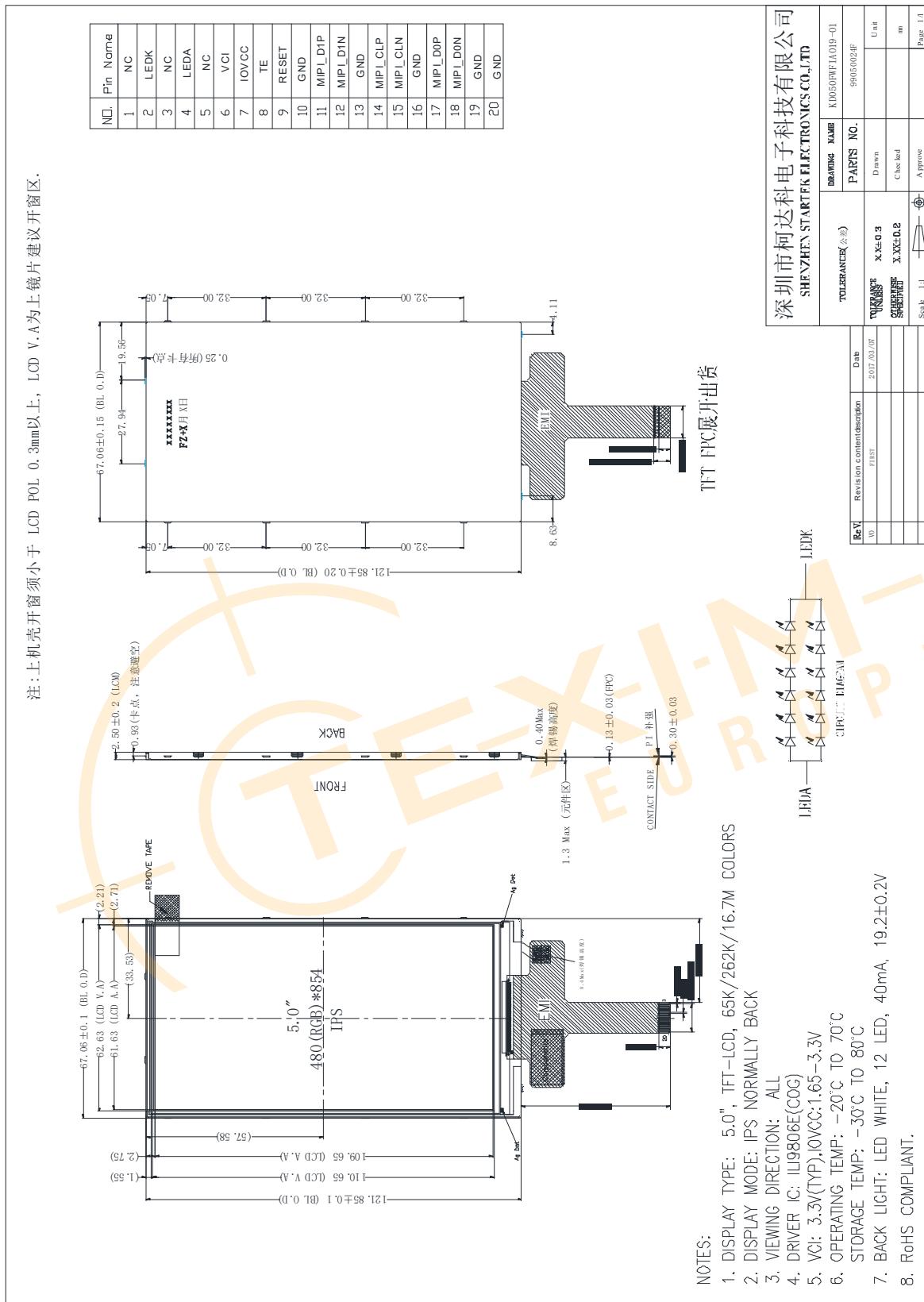
1. Block Diagram



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2. Outline dimension



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3. Input terminal Pin Assignment

3.1 TFT PIN Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	NC		
2	LEDK	Cathode pin of backlight.	P
3	NC		
4	LEDA	Anode pin of backlight.	P
5	NC		
6	VCI	Supply Voltage (3.3V).	P
7	IOVCC	I/O power supply voltage.	P
8	TE	-Tearing effect output Leave the pin to open when not in use.	O
9	RESET	- The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.	I
10	GND	Ground.	P
11	MIPI_D1P	MIPI DSI differential data pair (DSI-Dn+/-). If MIPI are not used, they should be connected to DGND	I/O
12	MIPI_D1N		I/O
13	GND	Ground.	P
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK+/-). If MIPI are not used, they should be connected to DGND.	I
15	MIPI_CLN		I
16	GND	Ground.	P
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn+/-). If MIPI are not used, they should be connected to DGND	I/O
18	MIPI_D0N		I/O
19	GND	Ground.	P
20	GND	Ground.	P

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4. LCD Optical Characteristics

4.1 Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note	
Contrast Ratio	CR	$\Theta=0$ Normal viewing angle	600	800	--		*(1)(2)	
Response time	Rising		--	16	21	msec	*(1)(3)	
	Falling		--	19	24			
Color gamut	S(%)		--	62	--	%	*	
Color Filter Chromacity	White	$\Theta=0$ Normal viewing angle	W _X	0.290	+0.04	-	*(1) (4) CA-310 Test	
			W _Y	0.322				
	Red		R _X	0.642				
			R _Y	0.346				
	Green		G _X	0.320				
			G _Y	0.616				
	Blue		B _X	0.142				
			B _Y	0.079				
Viewing angle	Hor.	Θ_L Θ_R	--	80	--	-	*(1) (4)	
			--	80	--			
	Ver.		Θ_U	80	--			
			Θ_D	80	--			
Option View Direction		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

Ambient temperature : $25 \pm 2^\circ\text{C}$

15min. warm-up time.

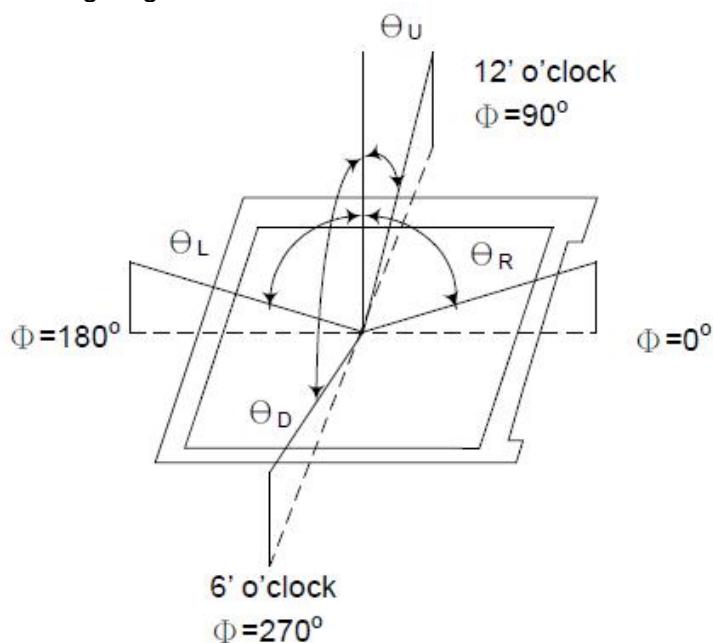
Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

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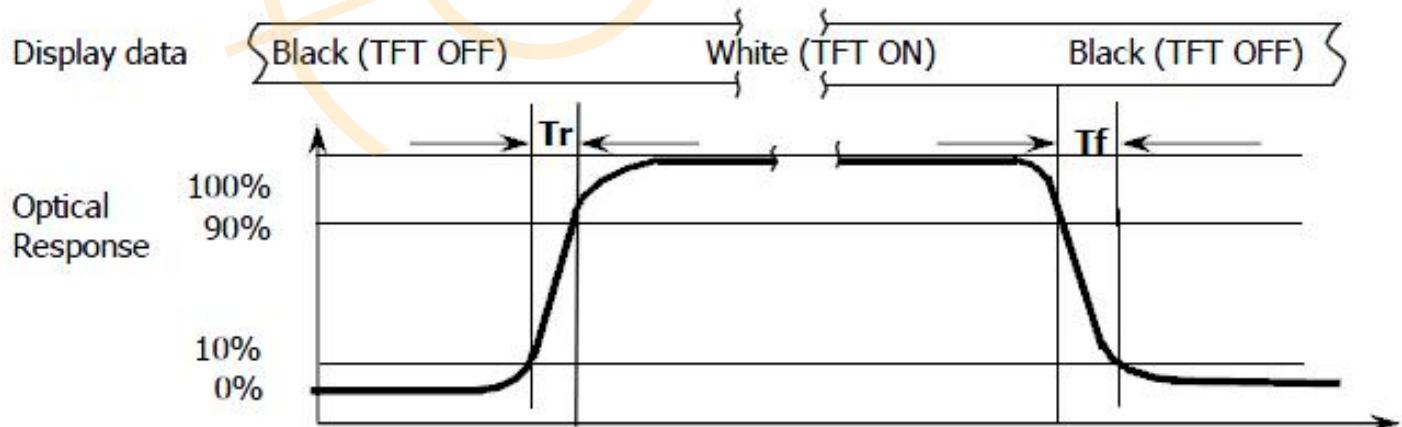
Note (1): Definition of Viewing Angle :



Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

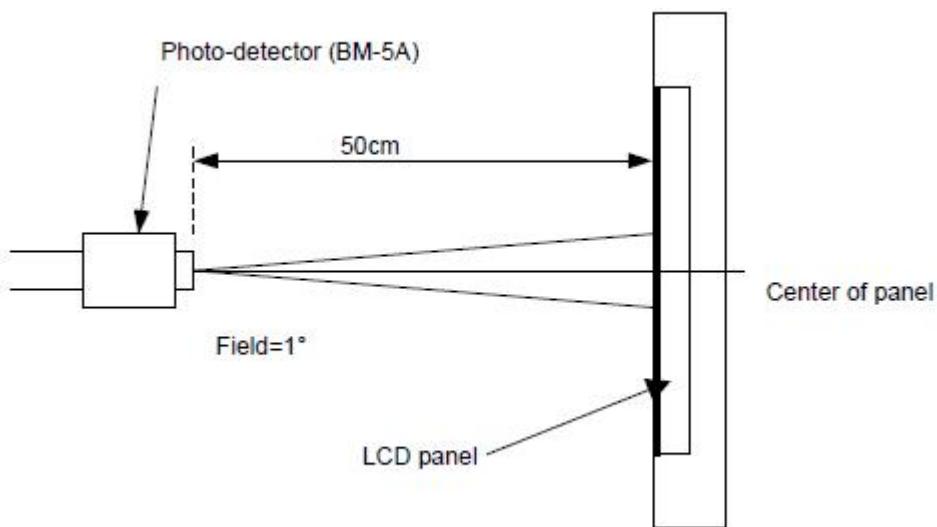
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



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Note (4): Definition of optical measurement setup



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5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	V _{CI}	-0.3	6.5	V
Digital interface supple Voltage	I _{OVCC}	-0.3	3.3	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	2.5	3.3	6.0	V	--
Digital interface supple Voltage	I _{OVCC}	1.65	1.8	3.3	V	--
Normal mode Current consumption	I _{DD}	--	40	80	mA	--
Level input voltage	V _{IH}	0.7 I _{OVCC}	--	I _{OVCC}	V	--
	V _{IL}	-0.3	--	0.3 I _{OVCC}	V	--
Level output voltage	V _{OH}	0.8* I _{OVCC}	--	I _{OVCC}	V	--
	V _{OL}	GND	--	0.2 I _{OVCC}	V	--



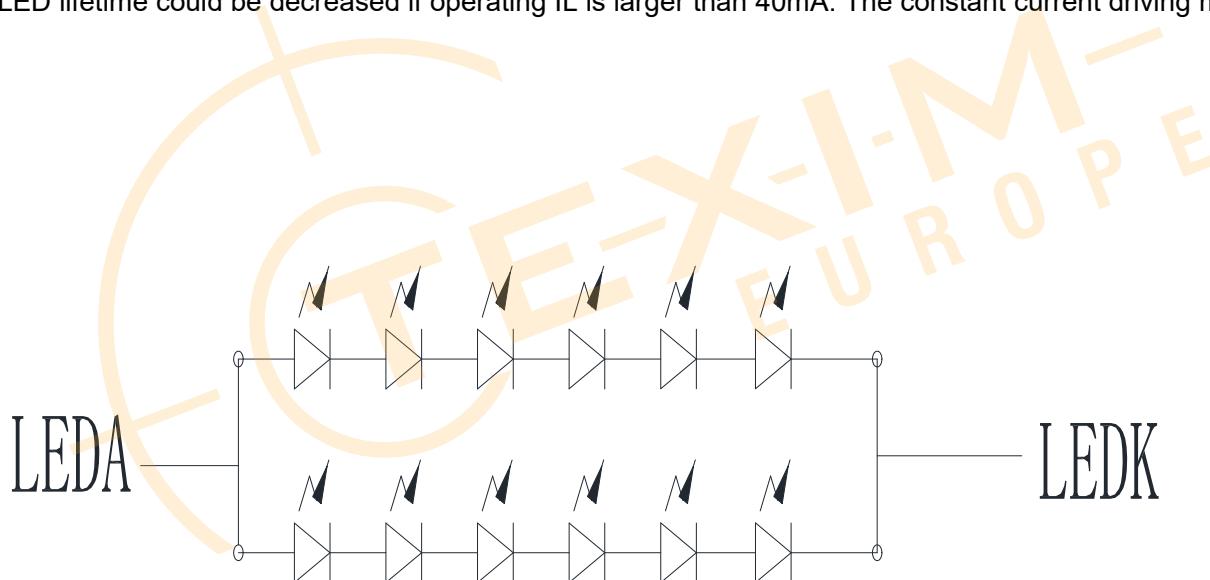
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 12 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	30	40	--	mA	--
Forward Voltage	V_F	--	19.2	--	V	--
LCM Luminance	L_V	350	400	--	cd/m ²	Note3
LED life time	Hr	50000			Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: $T_a=25\pm3$ °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

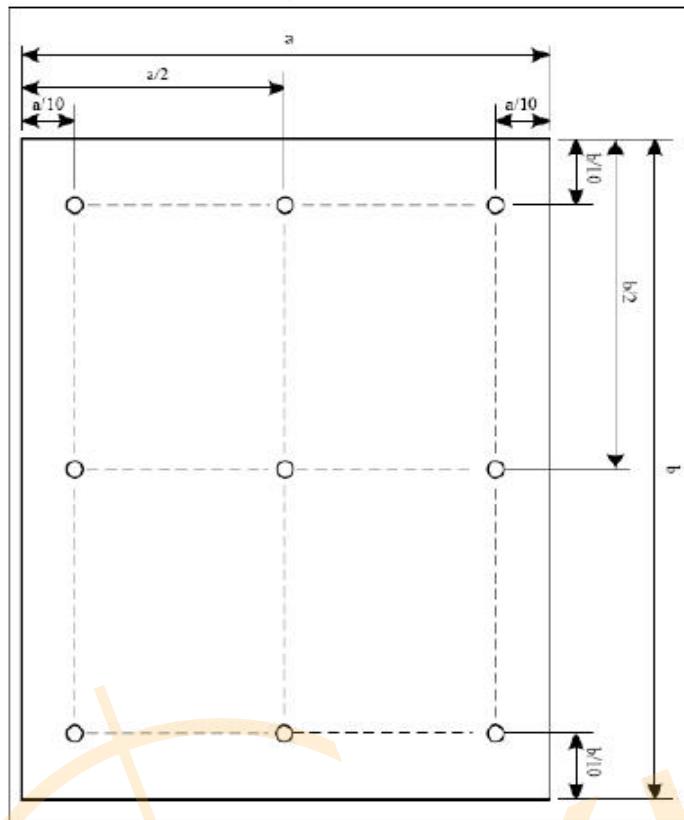
Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at $T_a=25$ °C and $IL=40$ mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM



NOTE 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

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6. MIPI Interface Characteristics

6.1 High Speed Mode – Clock Channel Timing

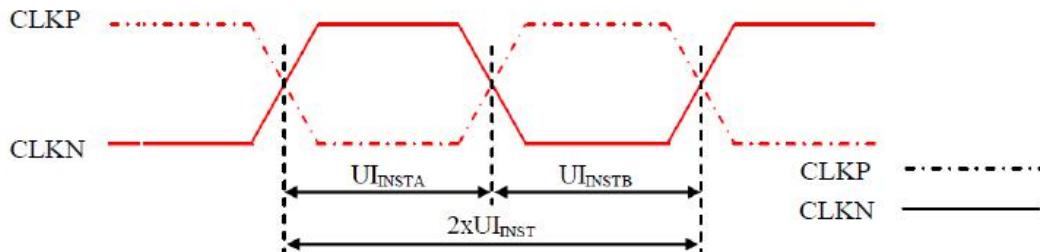


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. $UI = UI_{INSTA} = UI_{INSTB}$
2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps



6.2 High Speed Mode – Data Clock Channel Timing

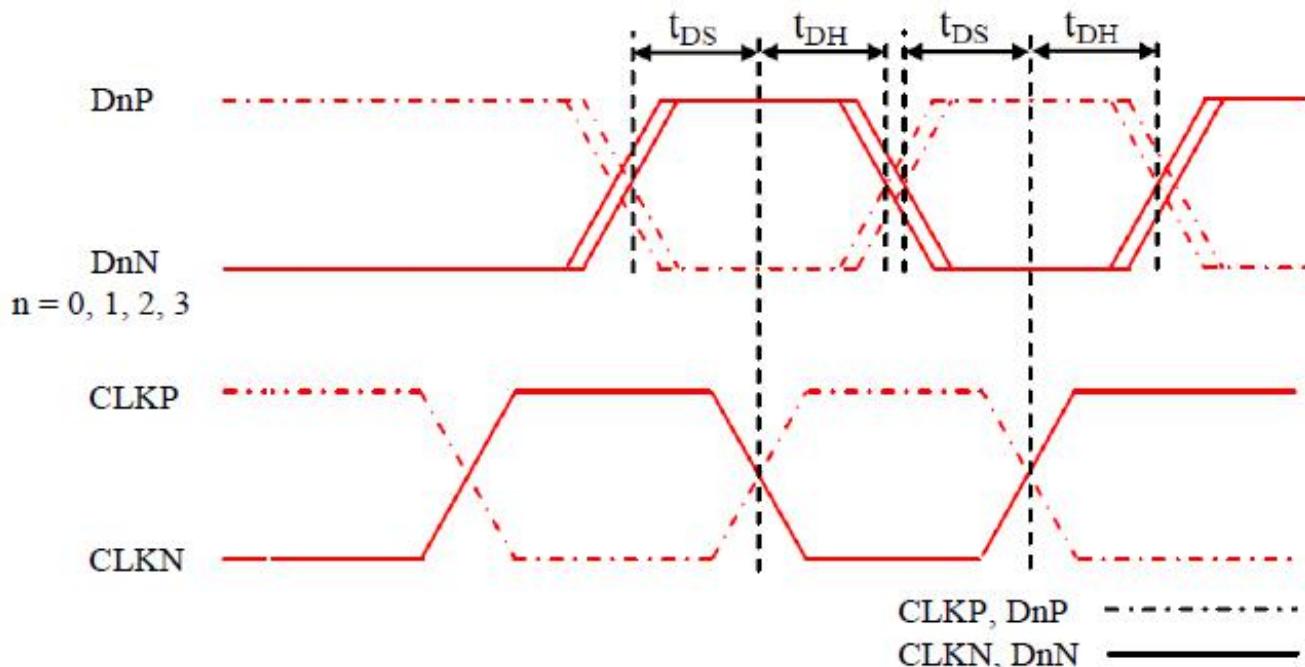


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-



6.3 High Speed Mode – Rising and Fall Timings

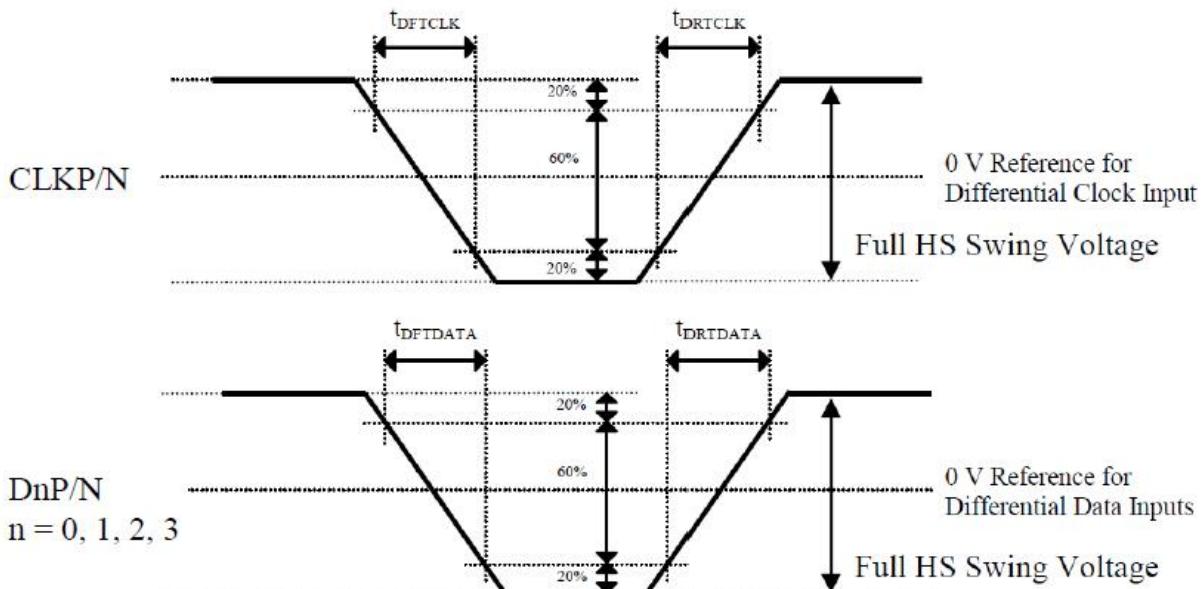


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N $n=0$ and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N $n=0$ and 1	150 ps	-	0.3UI (Note)

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.



6.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

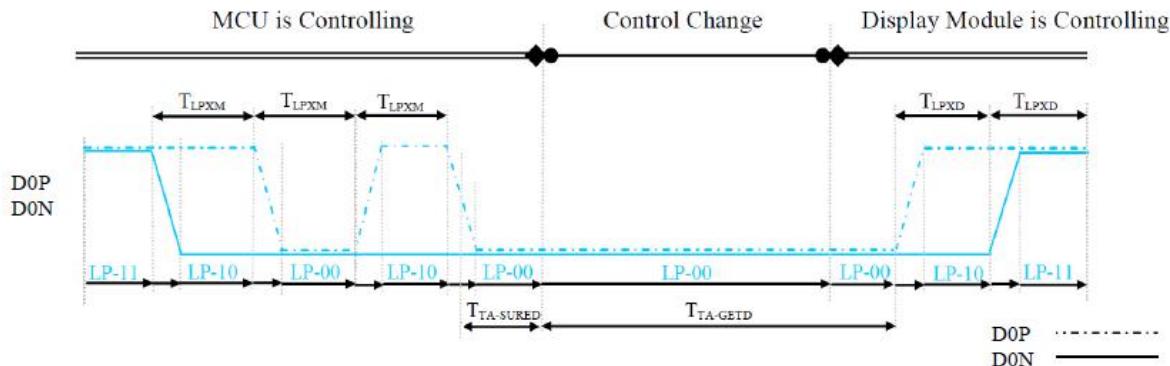


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

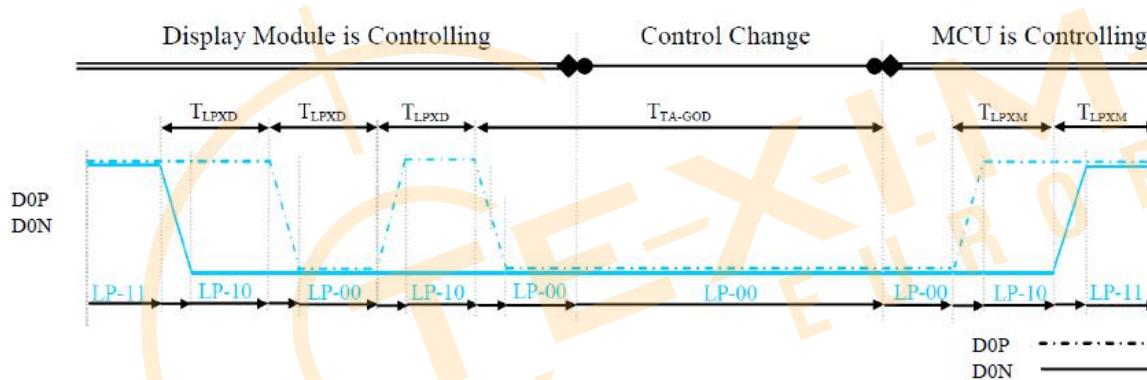


Figure 122: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5 \times T_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LPXD}$	ns

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6.5 Data Lanes from Low Power Mode to High Speed Mode

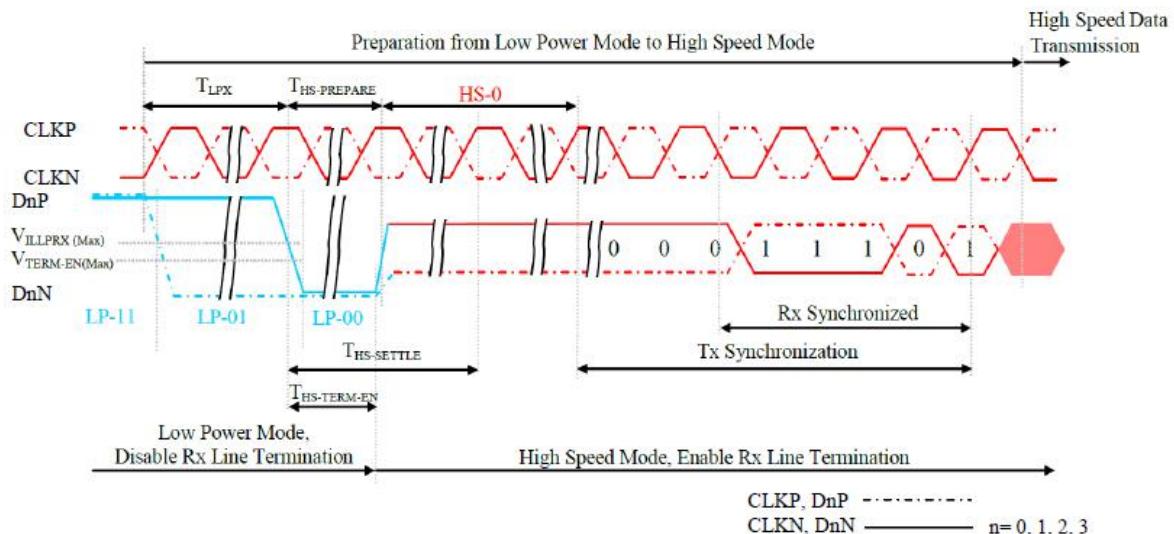


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses V_{ILMAX}	-	35+4xUI	ns



6.6 Data Lanes from High Power Mode to High Speed Mode

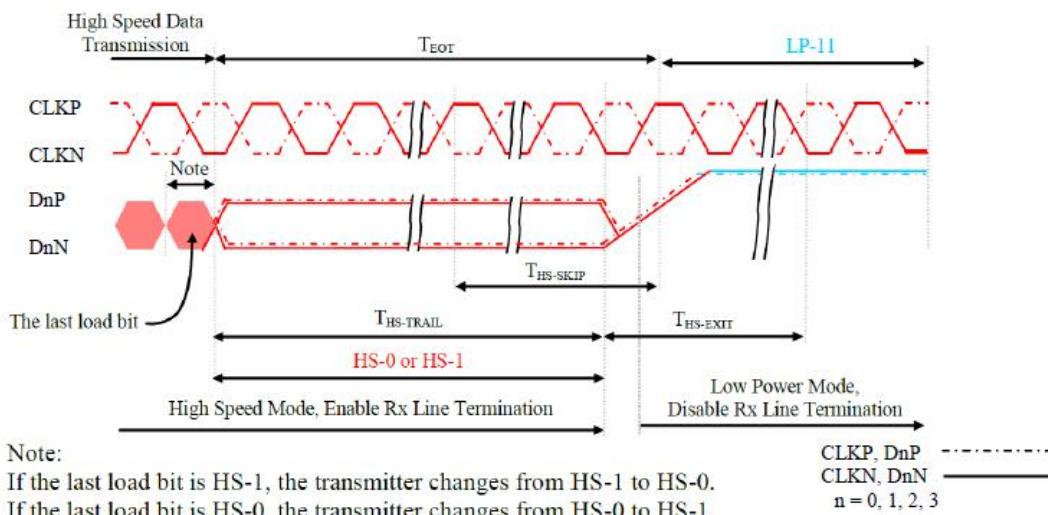


Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_HS-SKIP	Time-Out at Display Module (ILI9881C) to ignore transition period of Eot	40	55+4xUI	ns
DnP/N, n = 0 and 1	T_HS-EXIT	Time to driver LP-11 after HS burst	100	-	ns



6.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

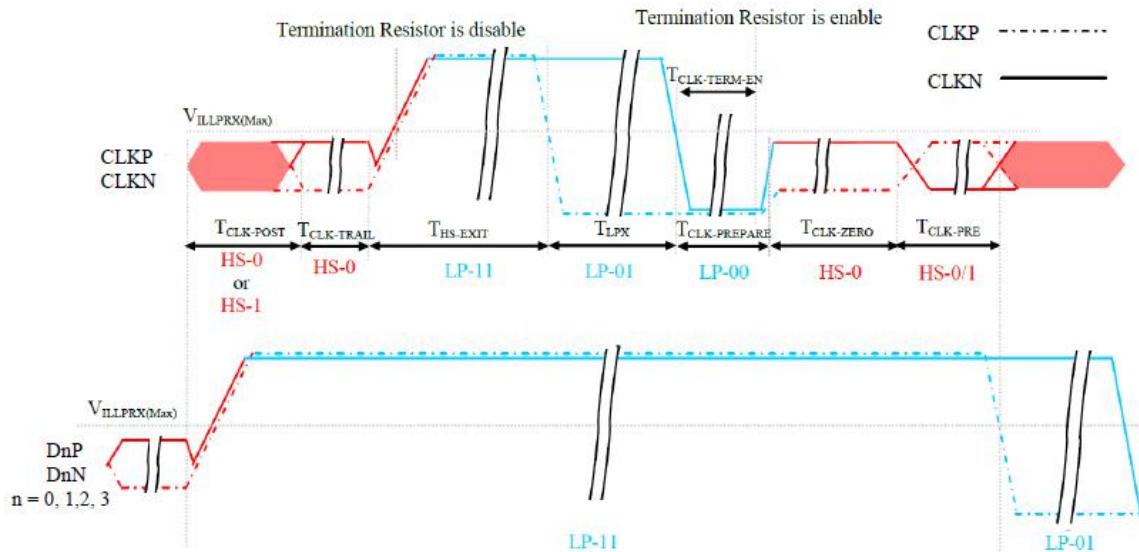


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	T _{CLK-POST}	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	T _{CLK-TRAIL}	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	T _{CLK-PREPARE}	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	T _{CLK-TERM-EN}	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	T _{CLK-PREPARE + T_{CLK-ZERO}}	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	T _{CLK-PRE}	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns



6.8 Timing for DSI video mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	(29)	--	MHz
Horizontal display area	HDISP	--	480	--	Clock
Horizontal Sync. Width	hpw	1	4	--	Clock
Horizontal Sync. Back Porch	hbp	1	30	-	Clock
Horizontal Sync. Front Porch	hfp	1	18	--	Clock
Vertical display area	VDISP	--	854	--	Line
Vertical Sync. Width	vs	1	4	--	Line
Vertical Sync. Back Porch	vbp	1	30	--	Line
Vertical Sync. Front Porch	vfp	1	20	--	Line
Frame-Rate		--	60	--	Hz



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6.9 Reset input timing

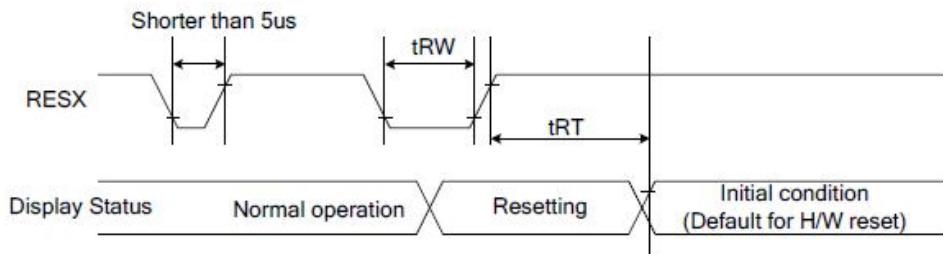


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	t_{RW}	Reset pulse duration	10		μs
	t_{RT}	Reset cancel		5 (note 1,5) 120 (note 1,6,7)	ms

Notes:

1. The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

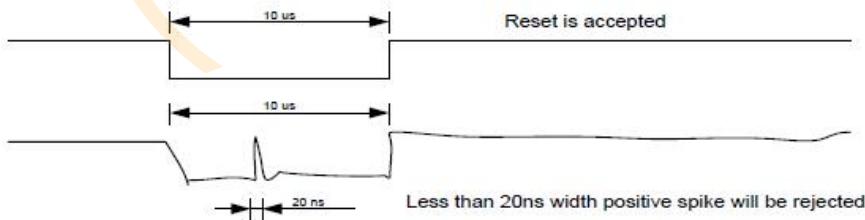


Figure 127: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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7.LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

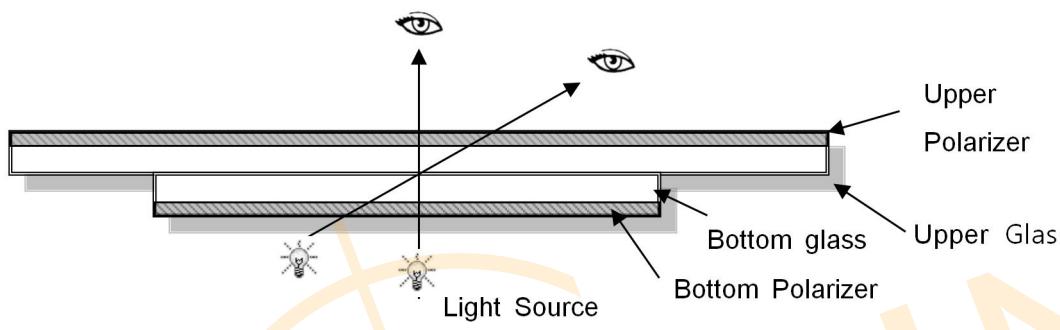
Temperature : $25\pm5^{\circ}\text{C}$

Humidity : $65\%\pm10\%\text{RH}$

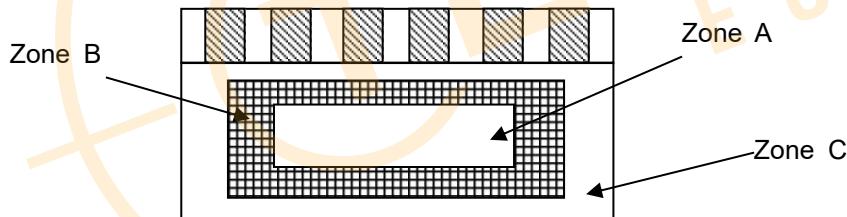
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

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7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module, CTP: Capacitive Touch Panel

No	Items to be inspected	Criteria	Classification of defect s
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc	Major
2	Missing	Missing components and etc	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc	Minor
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

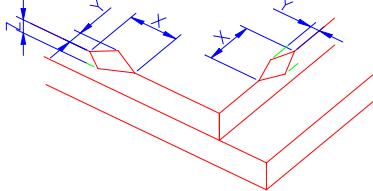
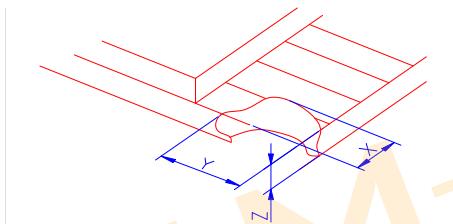
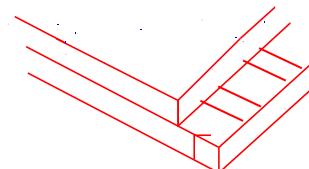
Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

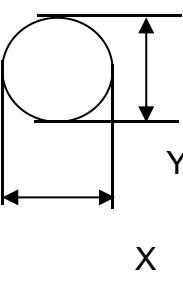
Part. No	KD050FWFIA019-01	REV	V1.0	Page 24 of 31
常备库存	Stock For Sale	长期供货	支持小量 NO MOQ	品种齐全 In Full Range



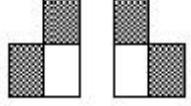
7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of IT O, T: Height of LCD	(1) The edge of LCD broken	 <table border="1"> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> <tr> <td>$\leq 3.0\text{mm}$</td> <td><Inner border line of the seal</td> <td>$\leq T$</td> </tr> </table>	X	Y	Z	$\leq 3.0\text{mm}$	<Inner border line of the seal	$\leq T$
X	Y	Z						
$\leq 3.0\text{mm}$	<Inner border line of the seal	$\leq T$						
	(2)LCD corner broken	 <table border="1"> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> <tr> <td>$\leq 3.0\text{mm}$</td> <td>$\leq L$</td> <td>$\leq T$</td> </tr> </table>	X	Y	Z	$\leq 3.0\text{mm}$	$\leq L$	$\leq T$
X	Y	Z						
$\leq 3.0\text{mm}$	$\leq L$	$\leq T$						
	(3) LCD crack	 <p>Crack Not allowed</p>						



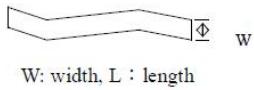
 <p>$\Phi = (X+Y)/2$</p>	<p>① light dot (black/white spot , pinhole, stain, etc.)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr> <tr> <th>A</th><th>B</th><th>C</th></tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.15$</td><td>Ignore</td><td colspan="2" rowspan="3">Ignore</td></tr> <tr> <td>$0.15 < \Phi \leq 0.25$</td><td>3(distance $\geq 10\text{mm}$)</td></tr> <tr> <td>$0.25 < \Phi \leq 0.4$</td><td>2(distance $\geq 10\text{mm}$)</td></tr> <tr> <td>$\Phi > 0.4$</td><td>0</td><td colspan="2" rowspan="3"></td></tr> </tbody> </table>				Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.15$	Ignore	Ignore		$0.15 < \Phi \leq 0.25$	3(distance $\geq 10\text{mm}$)	$0.25 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)	$\Phi > 0.4$	0			
Zone Size (mm)	Acceptable Qty																							
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$\Phi > 0.4$	0																							
<p>② Dim spot (light leakage、dent、dark spot, etc)</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr> <tr> <th>A</th><th>B</th><th>C</th></tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.15$</td><td>Ignore</td><td colspan="2" rowspan="3">Ignore</td></tr> <tr> <td>$0.15 < \Phi \leq 0.25$</td><td>3(distance $\geq 10\text{mm}$)</td></tr> <tr> <td>$0.25 < \Phi \leq 0.4$</td><td>2(distance $\geq 10\text{mm}$)</td></tr> <tr> <td>$\Phi > 0.4$</td><td>0</td><td colspan="2" rowspan="3"></td></tr> </tbody> </table>				Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.15$	Ignore	Ignore		$0.15 < \Phi \leq 0.25$	3(distance $\geq 10\text{mm}$)	$0.25 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)	$\Phi > 0.4$	0				
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<p>③ Polarizer accidented spot</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr> <tr> <th>A</th><th>B</th><th>C</th></tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.2$</td><td>Ignore</td><td colspan="2" rowspan="2">Ignore</td></tr> <tr> <td>$0.2 < \Phi \leq 0.5$</td><td>2(distance $\geq 10\text{mm}$)</td></tr> <tr> <td>$\Phi > 0.5$</td><td>0</td><td colspan="2" rowspan="3"></td></tr> </tbody> </table>				Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.2$	Ignore	Ignore		$0.2 < \Phi \leq 0.5$	2(distance $\geq 10\text{mm}$)	$\Phi > 0.5$	0						
Zone Size (mm)	Acceptable Qty																							
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<p>④ Polarizer Bubble</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr> <tr> <th>A</th><th>B</th><th>C</th></tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.2$</td><td>Ignore</td><td colspan="2" rowspan="2">Ignore</td></tr> <tr> <td>$0.2 < \Phi \leq 0.4$</td><td>2(distance $\geq 10\text{mm}$)</td></tr> <tr> <td>$\Phi > 0.4$</td><td>0</td><td colspan="2"></td></tr> </tbody> </table>				Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.2$	Ignore	Ignore		$0.2 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)	$\Phi > 0.4$	0						
Zone Size (mm)	Acceptable Qty																							
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$\Phi \leq 0.2$	Ignore	Ignore																						
$0.2 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)																							
$\Phi > 0.4$	0																							



3.0	LCD Pixel defect	Pixel bad points	Item	Zone A	Acceptable Qt				
			Bright dot	Random	N≤2				
				2 dots adjacent	N≤0				
				3 dots adjacent	N≤0				
			Dark dot	Random	N≤3				
				2 dots adjacent	N≤0				
				3 dots adjacent	N≤0				
			Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm				
				Total bright and dark dot					
			Note:						
A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.									
B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.									
C) 2 dot adjacent = 1 pair = 2 dots									
Picture:									
 2 dot adjacent			 2 dot adjacent						
 2 dot adjacent (vertical)			 2 dot adjacent (slant)						



SHENZHEN STARTEK ELECTRONIC TECHNOLOGY CO. , LTD

4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)  N : Count	<table border="1"> <thead> <tr> <th rowspan="2">Width(mm)</th><th rowspan="2">Length(m)</th><th colspan="3">Acceptable Qty</th></tr> <tr> <th>A</th><th>B</th><th>C</th></tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.05$</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr> <tr> <td>$0.05 < W \leq 0.06$</td><td>$L \leq 5.0$</td><td colspan="3">$N \leq 3$</td></tr> <tr> <td>$0.06 < W \leq 0.08$</td><td>$L \leq 4.0$</td><td colspan="3" rowspan="2">$N \leq 2$</td></tr> <tr> <td>$W > 0.08$</td><td colspan="4">Define as spot defect</td></tr> </tbody> </table>	Width(mm)	Length(m)	Acceptable Qty			A	B	C	$\Phi \leq 0.05$	Ignore	Ignore		Ignore	$0.05 < W \leq 0.06$	$L \leq 5.0$	$N \leq 3$			$0.06 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$			$W > 0.08$	Define as spot defect			
Width(mm)	Length(m)	Acceptable Qty																												
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$0.06 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$																												
$W > 0.08$	Define as spot defect																													
5.0	Electronic Components SMT.	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite																												
6.0	Display color& Brightness.	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.																												
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.																												

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	CTP no function	Not allowed



8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70°C, 96H	
Low Temperature Operating	-20°C, 96HR	
High Temperature Storage	80°C, 96HR	Inspection after 2~4hours
Low Temperature Storage	-30°C, 96HR	storage at room temperature, the
High Temperature & High Humidity Operating	+60°C, 90% RH ,96 hours.	sample shall be free from defects:
Thermal Shock (Non-operation)	-20°C,30 min ↔ +70°C,30 min, Change time:5min 20CYC.	1.Air bubble in the LCD; 2.Non-display;
ESD test	C=150pF , R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

Part. No	KD050FWFIA019-01	REV	V1.0	Page 29 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	



9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

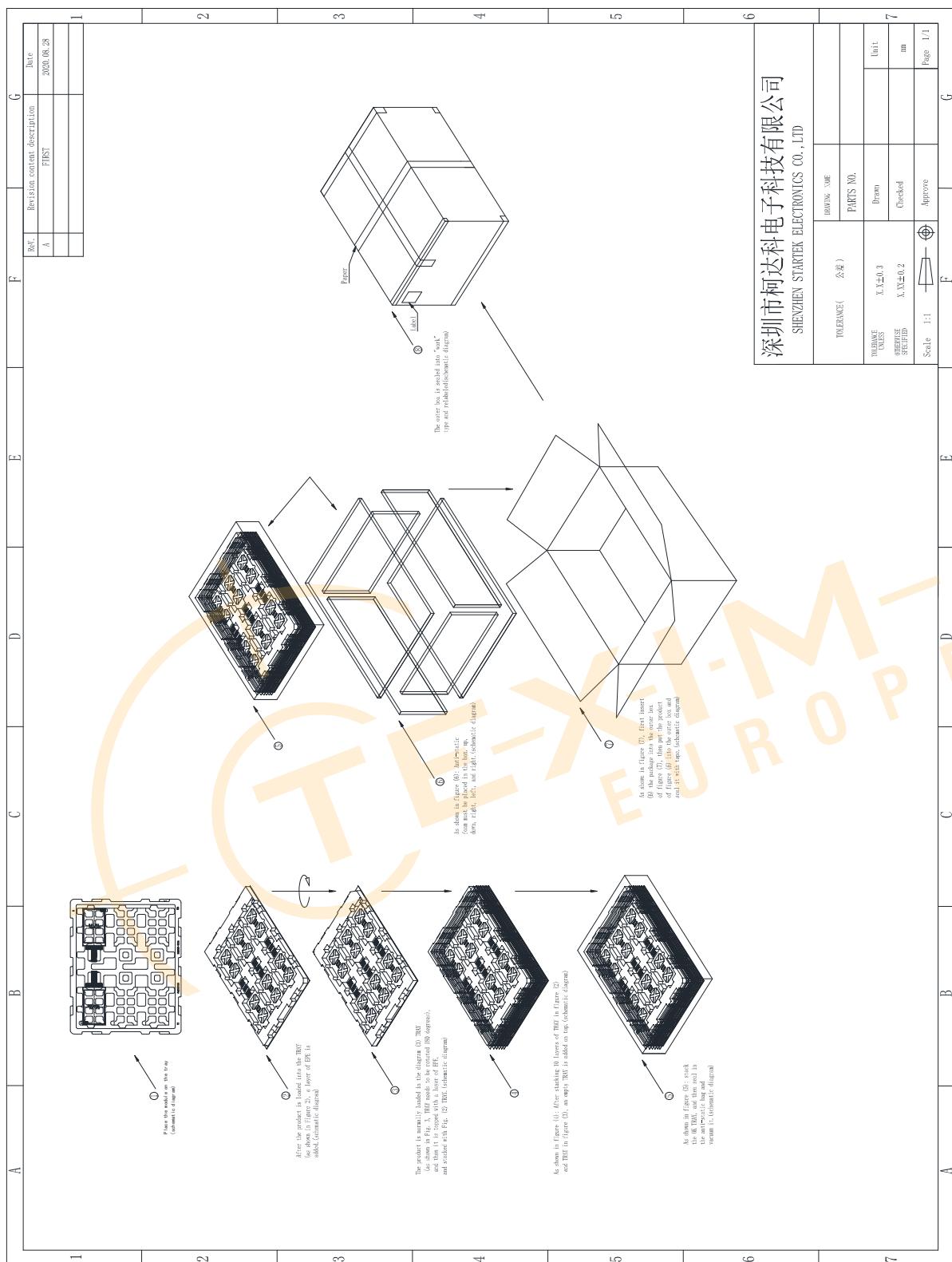
9.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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10. Packing



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常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

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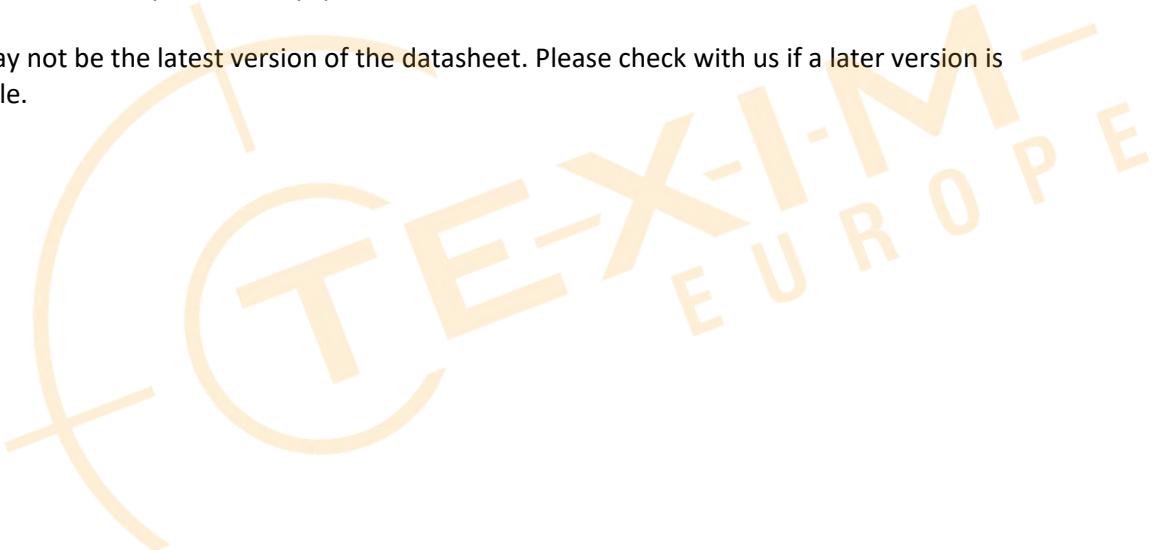
It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application.

Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time.

All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts.

Please contact us if you have any questions about the contents of the datasheet.

This may not be the latest version of the datasheet. Please check with us if a later version is available.





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