Shenzhen Leadtek Electronics Co.,Ltd

PRODUCT SPECIFICATION

TFT-LCD MODULE

Module No：LTK100UXHLM10-V0

☑ Preliminary Specification

☐ Approval Specification

Designed by	Checked by	Approved by
jona	Jerry	lan

Final Approval by Customer

Approved by	Comment
	Distributed by: TEXIM EUROPE www.texim-europe.com

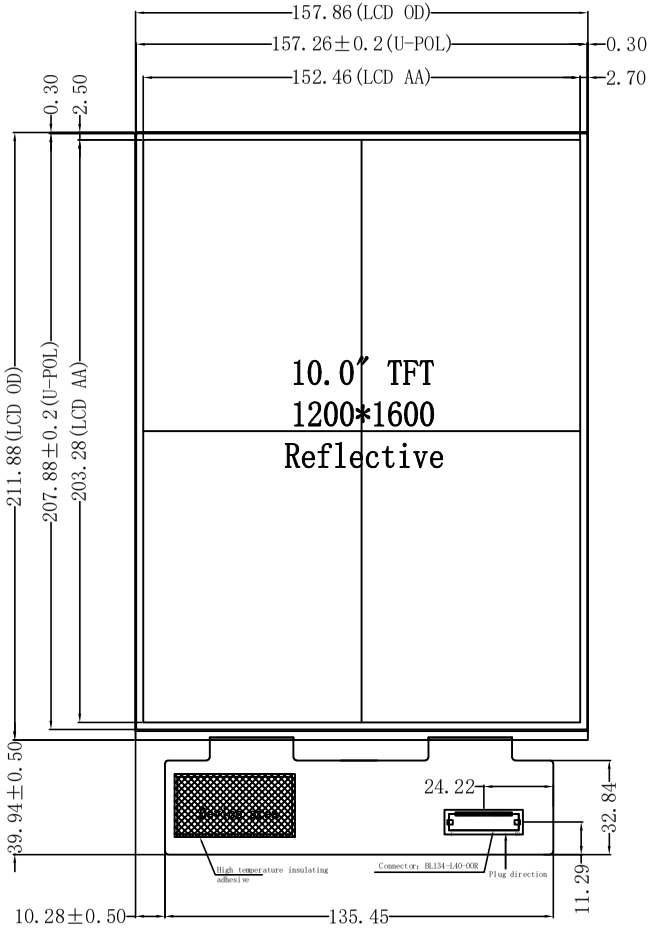
※The specification of “TBD” should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.

2. General Description

N0	Item	Specification	Unit	Remark
1	LCD Size	TFT"10	inch	-
2	Panel Type	a-silicon	-	-
4	Number of pixels	1200 x RGB x 1600	pixel	-
5	Display mode	Normally White Reflective	-	-
6	Display colors	16.7M	-	-
7	Viewing Direction	60° / 60° / 60° / 60° (CR > 2)	-	-
8	LCM Module Size	157.86(H)x 211.88(V) x 0.72 (T)	mm	Note
9	Active Area	152.46 (W) x 203.28 (L)	mm	Note
10	Pixel Pitch	0.12705 (H) x 0.12705 (V)	mm	-
11	Weight	TBD	g	-
12	Driver IC	HX8279D	bit	-
13	Light Source	-	-	-
14	Interface	MIPI 4 Lanes	-	-

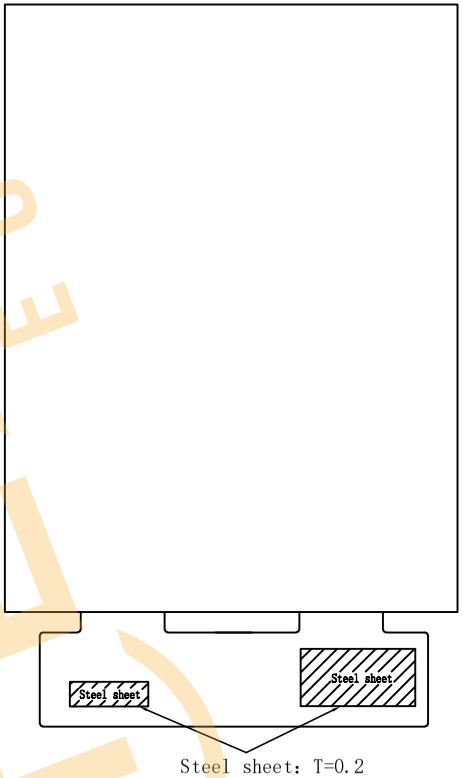
3. Mechanical Drawing

Front View



Side View

Back View



PIN	SYMBOL
1	IOVCC
2	VDDIN
3	VDDIN
4	GND
5	RESET
6	NC
7	GND
8	MIPI_DON
9	MIPI_DOP
10	GND
11	MIPI_D1N
12	MIPI_D1P
13	GND
14	MIPI_CKN
15	MIPI_CKP
16	GND
17	MIPI_D2N
18	MIPI_D2P
19	GND
20	MIPI_D3N
21	MIPI_D3P
22	GND
23	NC
24	NC
25	GND
26	NC
27	NC
28	NC
29	NC
30	GND
31	LEDK
32	LEDK
33	NC
34	ID
35	NC
36	NC
37	NC
38	NC
39	LEDA
40	LEDA

Notes:
1. Display : 10.0″, TFT
2. Resolution: 1200xRGBx1600
3. LCD Viewing Direction: 60/60/60/60
4. Drive IC:HX8279D+HX8279D
5. Display Mode: Normally White/Reflective
6. unmark Tolerance:±0.2
7. OPERATING TEMP: -20° C~ +70° C
8. STORAGE TEMP: -30° C~ +80° C
9. Requirements on Environmental Protection: ROHS

REV	DESCRIPTION	DATE	NAME
3			
2			
1			
0	NEW	2023.07.19	IAN

LEADTEK COMPANY LIMITED

SCALE:1/1	UNIT:mm	PAGE:1/1		Approve	Check	Drawn
Part No:	LTK100UXHLM10		VER:V0		JONA	IAN
Customer No:						

4. Interface Pin Connection

PIN NO	SYMBOL	DESCRIPTION
1	IOVCC	Power supply for the logic power and I/O circuit
2	VDDIN(3.3V)	Power Voltage for digital circuit 3.3V.
3	VDDIN (3.3V)	Power Voltage for digital circuit 3.3V.
4	GND	Ground.
5	Reset	Global reset pin.
6	NC	No connect.
7	GND	Ground.
8	MIPI_D0N	MIPI-D0Nare differential small amplitude signals.
9	MIPI_D0P	MIPI-D0Pare differential small amplitude signals.
10	GND	Ground.
11	MIPI_D1N	MIPI-D1Nare differential small amplitude signals.
12	MIPI_D1P	MIPI-D1Pare differential small amplitude signals.
13	GND	Ground.
14	MIPI_CLKN	MIPI-CLKNare differential small amplitude signals.
15	MIPI_CLKP	MIPI-CLKPare differential small amplitude signals.
16	GND	Ground.
17	MIPI_D2N	MIPI-D2Nare differential small amplitude signals.
18	MIPI_D2P	MIPI-D2Pare differential small amplitude signals.
19	GND	Ground.
20	MIPI_D3N	MIPI-D3Nare differential small amplitude signals.
21	MIPI_D3P	MIPI-D3Pare differential small amplitude signals.
22	GND	Ground.
23	NC	No connect.
24	NC	No connect
25	GND	Ground.
26	NC	No connect.
27	NC	No connect.
28	NC	No connect.
29	NC	No connect.
30	GND	Ground.
31	VLED-	Power for LED backlight (Cathode)
32	VLED-	Power for LED backlight (Cathode)
33	NC	No connect.
34	ID	ID PIN Pull High, If not use, please not connect.
35	NC	No connect.
36	NC	No connect.
37	NC	No connect.
38	NC	No connect.
39	VLED+	Power for LED backlight (Anode)
40	VLED+	Power for LED backlight (Anode)

5. 0 LCM DC CHARACTERISTICS

(Ta=25±2°C)

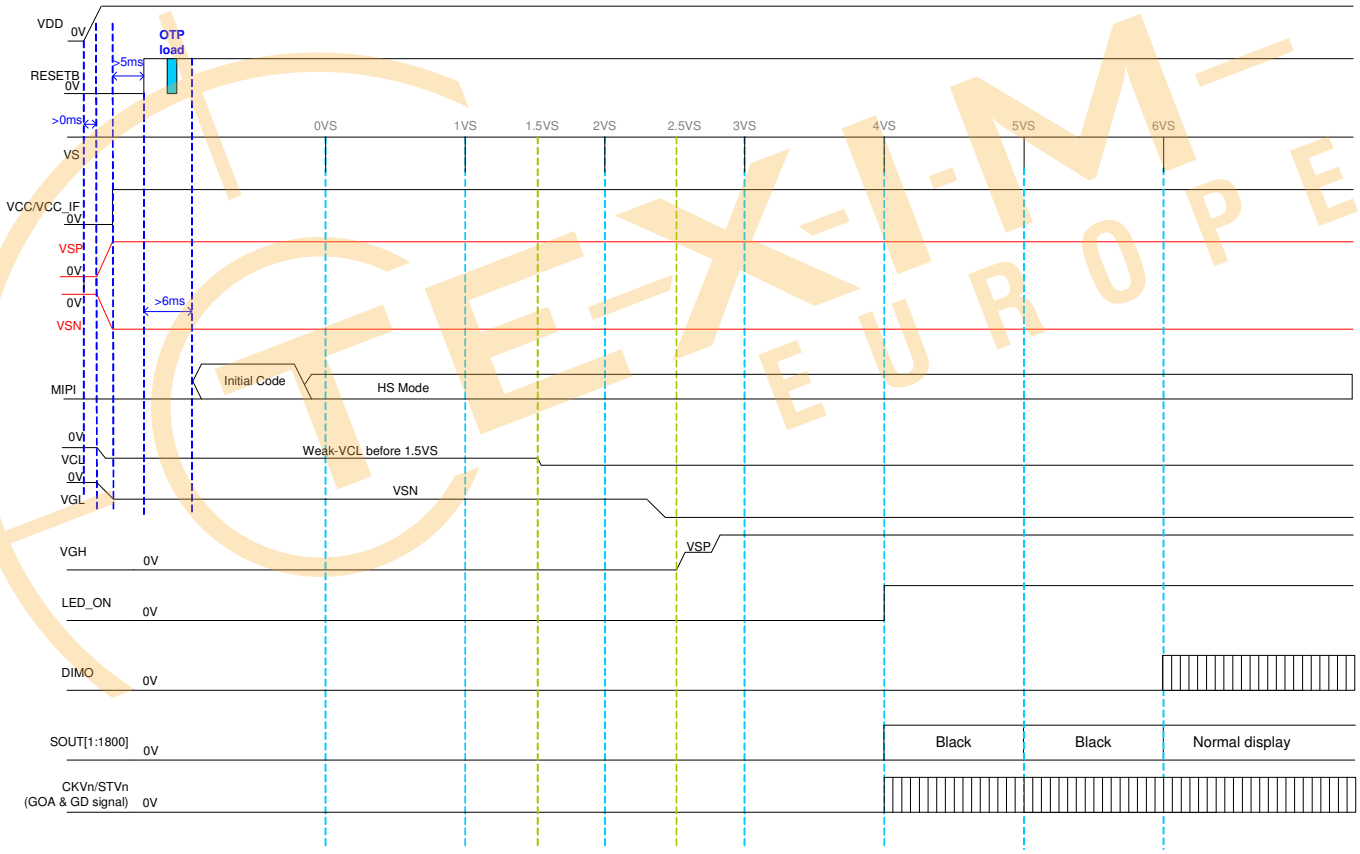
Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage 1	IOVCC	1.65	1.8	3.3	V	
Power Supply Voltage 2	VCI	2.5	2.8	3.6	V	

5.1 Power on/off sequence

5.1.1 Power on sequence PWRMD=0 ➔ Max. Power on time=7.0VS

After reset state or exit STB mode, the power on sequence will start.

To prevent the device from damage due to latch up, The VGL will be earlier than VGH. At 2.25VS the VGL negative high voltage will be generated via the external charge pump circuit. Then at 2.5VS the VGH positive high voltage can be generated via the external charge pump circuit. One SCHOTTKY diode is necessary between VGL and GND when VDD and VSP start at the same time.



Note: (1) Finish to write the GOA MUX (page1 registers) and GOA timing setting (page3 registers) within 50ms after reset pulls to high.

Figure 5.5: Power on sequence with PWRMD=0 and repair OP disable

5.1.2 Power off sequence PWRMD=0 ➔ Max. Power off time=5.0VS

When enter STB mode, the STBYB signal will be set to low. The power off sequence will start.

Power-off sequence
External VSP/VSN. Internal VGH/VGL.

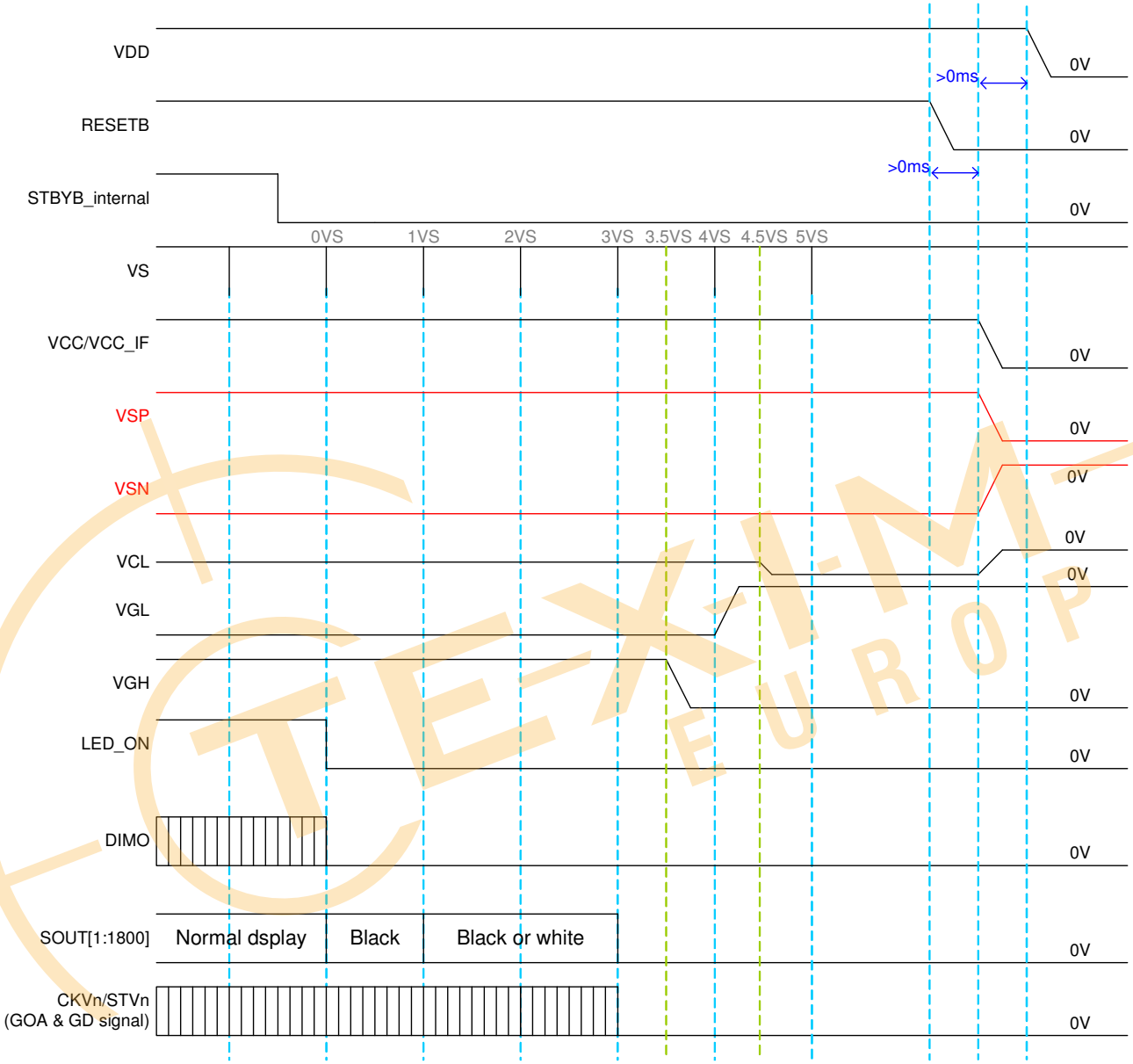
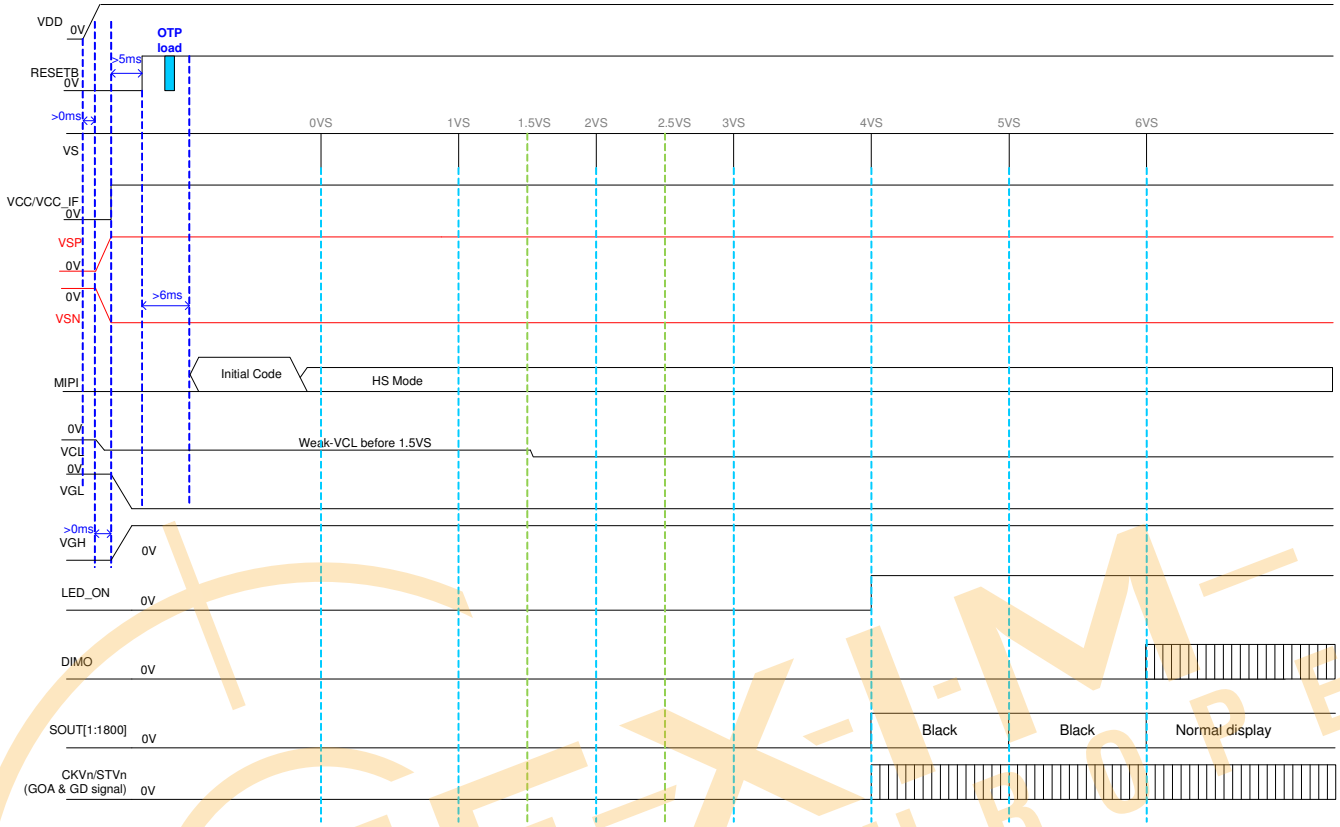


Figure 5.6: Power off sequence with PWRMD=0

5.1.3 Power on sequence PWRMD=1 ➔ Max. Power on time=6.0VS

After reset state or exit STB mode, the power on sequence will start. One SCHOTTKY diode is necessary between VGL and GND when VDD and VSP start at the same time.



Note: (1) Finish to write the GOA MUX (page1 registers) and GOA timing setting (page3 registers) within 50ms after reset pulls to high

Figure 5.7: Power on sequence with PWRMD=1 and repair OP disable

5.1.4 Power off sequence PWRMD=1 ➔ Max. Power off time=4.5VS

When enter STB mode, the STBYB signal will be set to low then the power off sequence will start.

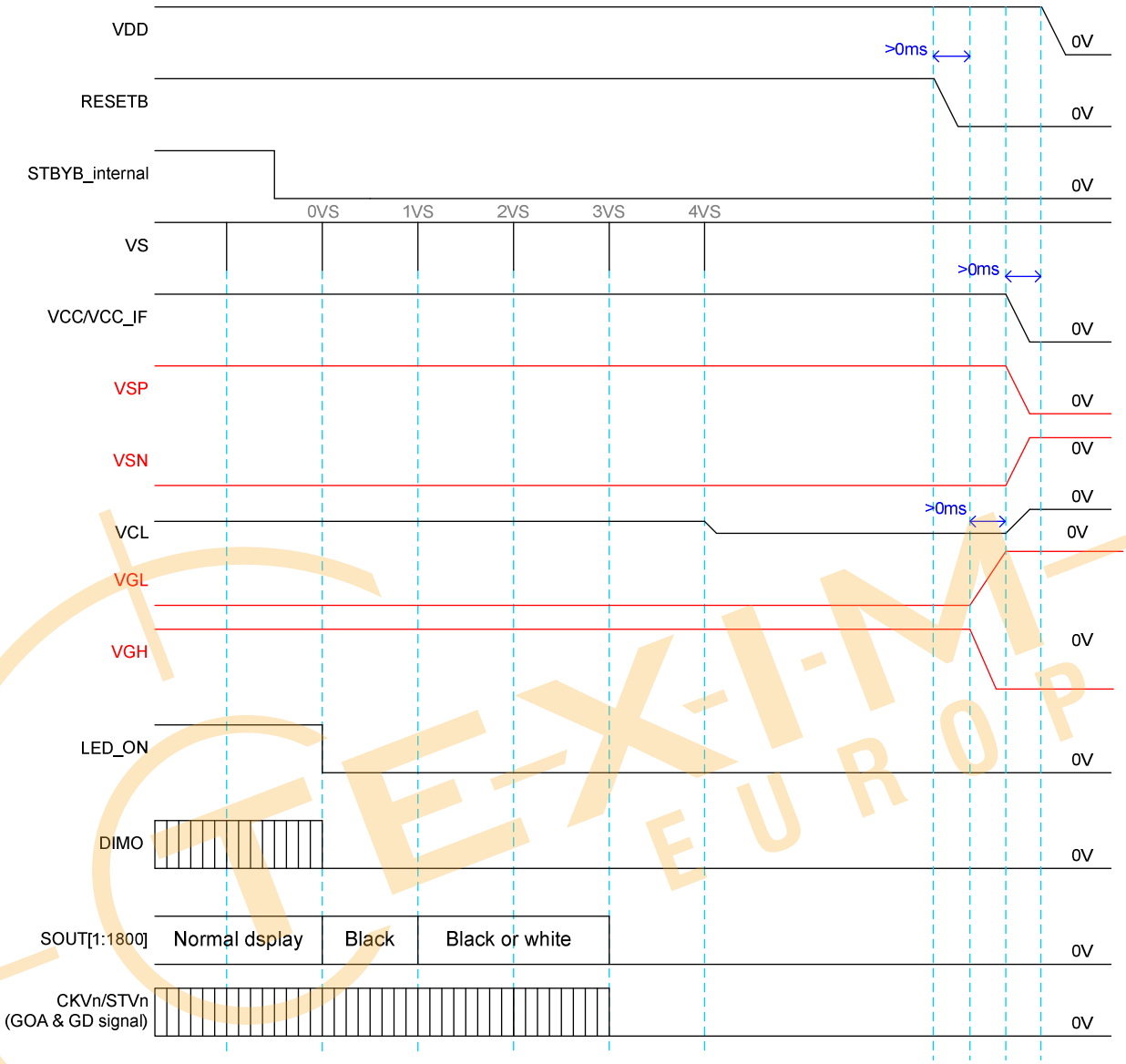


Figure 5.8: Power off sequence with PWRMD=1

6.0 AC Characteristics

6.1 MIPI AC characteristics

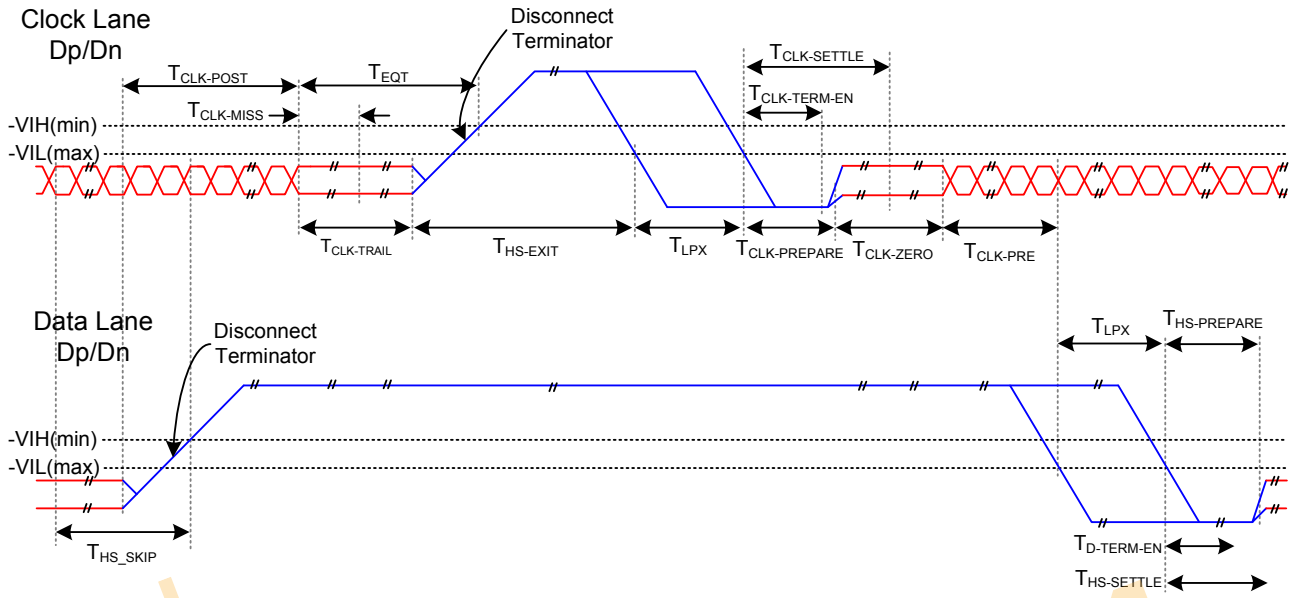


Figure 1: Switching the clock lane between clock transmission and low-power mode

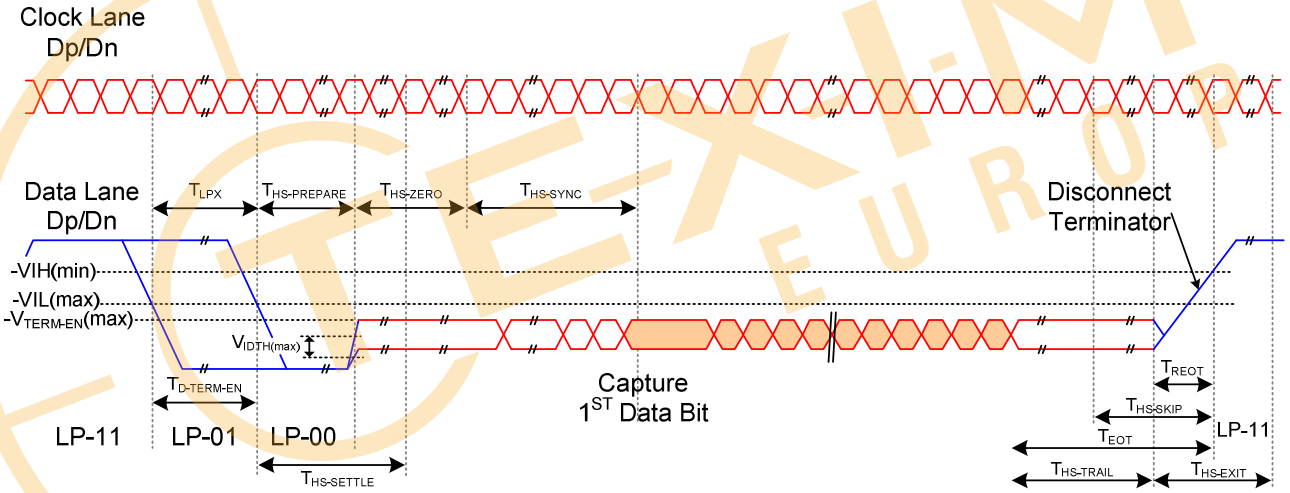


Figure .2: Timing of high-speed data transmission in bursts

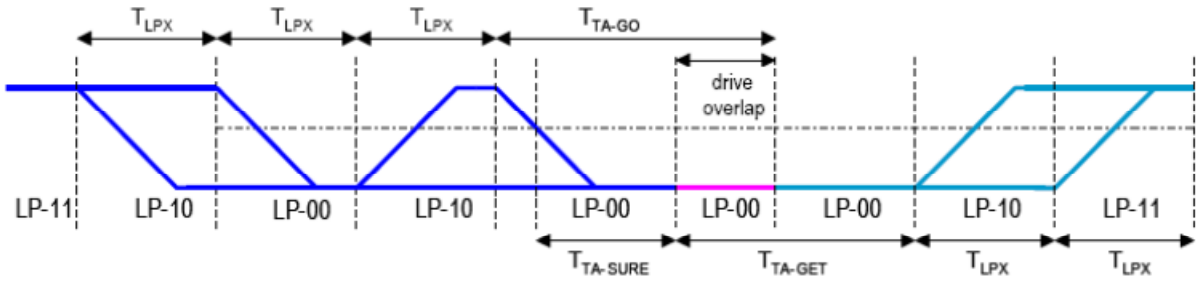


Figure 13.3: Turnaround Procedure

6.2 MIPI AC Characteristics

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI **(For DCS)**	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI		145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$ (1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

6.2.1 MIPI data-clock timing specification

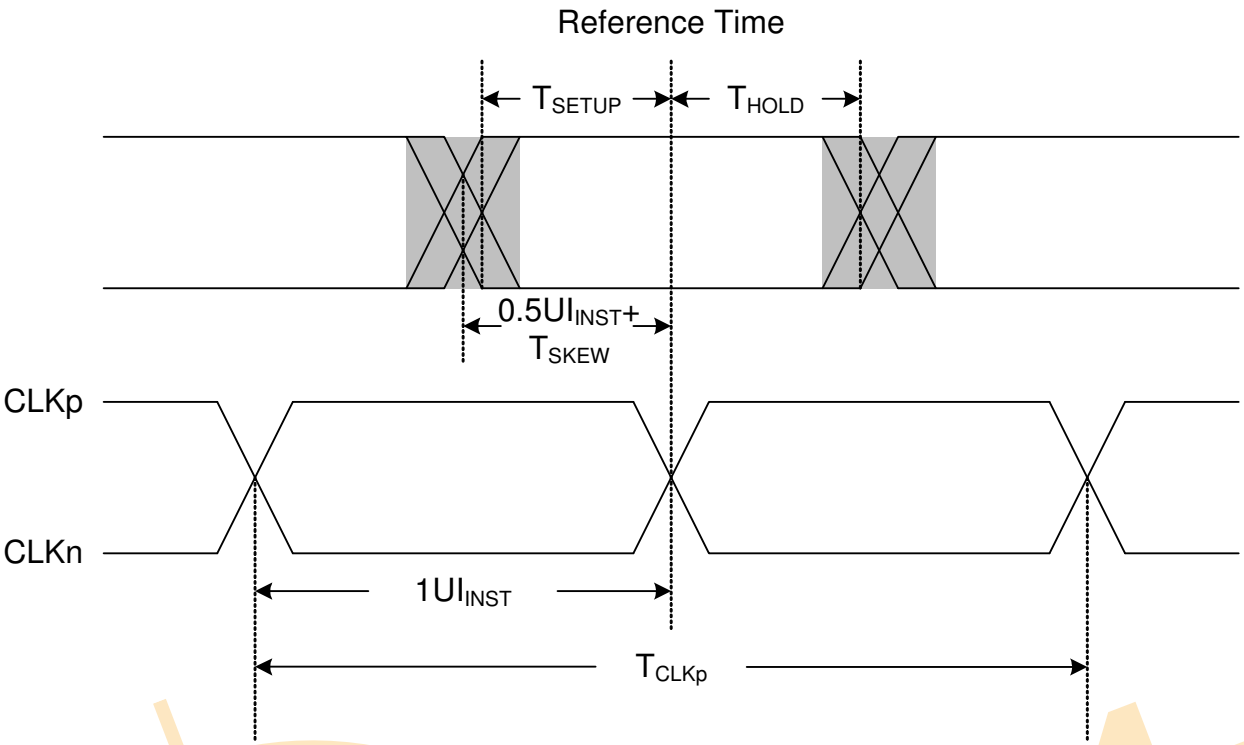


Figure 13.4: Data to clock timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous	UI_{INST}	1.0	-	12.5(1)	ns
Data to clock setup time	T_{SETUP}	0.3	-	-	UI_{INST}
Data to clock hold time	T_{HOLD}	0.3	-	-	UI_{INST}

Note: (1) This value corresponds to a minimum 80 Mbps data rate.

7.0 OPTICAL CHARACTERISTICS

7.1 Optical Specification (Reflective, w/Leadtek FOG+D65 light)

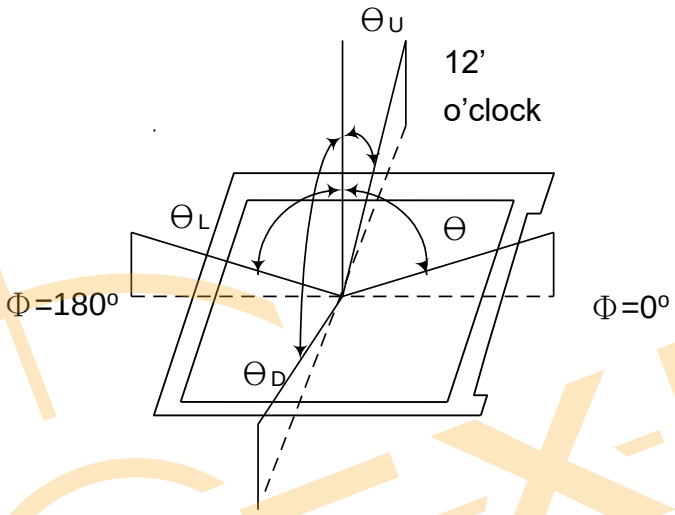
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
White Reflectance (with Polarizer)		Rw (%)	Θ=0 Normal viewing angle —	—	23	—	%	(4) Measuring with Leadtek Display polarizer ,Reference Only Base on Vop=4.5V
Contrast Ratio (CR>2)		CR		—	15	—	—	(1)(2) Base on Vop=4.5V
NCS		S(%)		—	35	—	%	Reflective
Response Time		ms			5	7		
Viewing Angle	Hor.	Θ_L	CR>2	—	60	—	—	(1)(4)Measuring with Leadtek Display polarizer ,Reference Only
		Θ_R		—	60	—		
	Ver.	Θ_U		—	60	—		
		Θ_D		—	60	—		

■ Measuring surrounding：dark room
■ Ambient temperature：25±2°C
■ 15min. warm-up time.

7.2 Measuring Equipment

■ DMS (DMS = Display Measurement System) of AUTRONIC-MELCHERS GmbH, motorized goniometer system for comprehensive display characterization

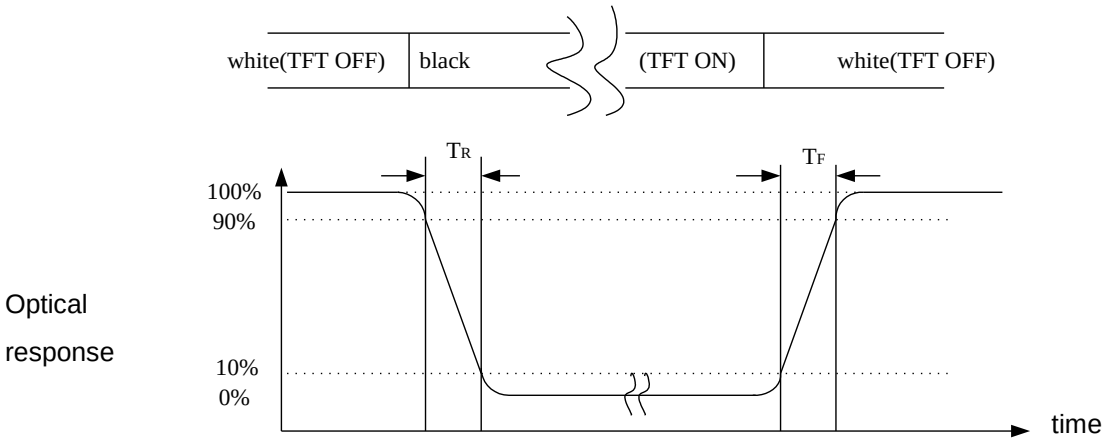
Note (1) Definition of Viewing Angle:



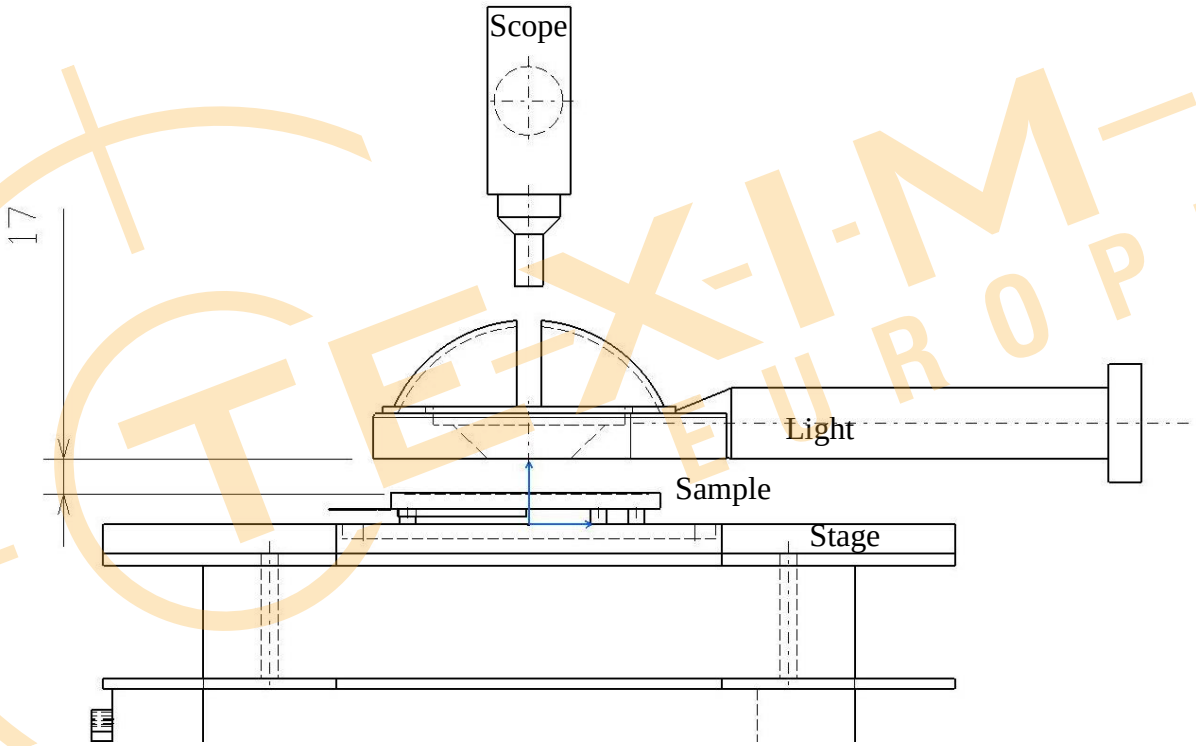
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



8. 0 RELIABILITY TEST ITEMS

No.	Item	Conditions	Remark
1	High Temperature Storage	Ta=+80°C, 240hrs	-
2	Low Temperature Storage	Ta=-30°C, 240hrs	-
3	High Temperature Operation	Ta=+70°C, 240hrs	-
4	Low Temperature Operation	Ta=-20°C, 240hrs	-
5	High Temperature and High Humidity (Operating)	Ta=+60°C, 90%RH, 240hrs	-

Note: (1) All tests above are practiced at module type.

(2) There is no display function NG issue occurred, all the cosmetic specification is judged before the reliability stress.

9.0 General Precaution

9.1 Use Restriction

9.2 Asembly Precaytton

1、Please use the mounting hole on the module side in installing and do not bending or wrenching LCD in assembling. And please do not drop, bend or twist LCD module in handling.

2、Please design display housing in accordance with the following guide lines.

3、Housing case must be destined carefully so as not to put stresses on LCD all sides and not to wrench module. The stresses may cause non-uniformity even if there is no non-uniformity statically.

4、Keep sufficient clearance between LCD module back surface and housing when the LCD module is mounted. The clearance in the design is recommended taking into account the tolerance of LCD module thickness and mounting structure height on the housing.

5、 Please do not push or scratch LCD panel surface with any-thing hard. And do not soil LCD panel surface by touching with bare hands. (Polarizer film, surface of LCD panel is easy to be flawed.)

6、Please do not press any parts on the rear side such as source IC, gate IC, and FPC during handling LCD module. If pressing rear part is unavoidable, handle the LCD module with care not to damage them.

7、Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.

8、 Please wipe out drops of adhesives like saliva and water on LCD panel surface immediately. They might damage to cause panel surface variation and color change.

9. Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.

9.3 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. Leadtek does not warrant the module, if customers disassemble or modify the module.

9.4 Breakage of LCD Panel

1 、If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

2、 If liquid crystal contacts mouth or eyes, rinse out with water immediately.

3、 If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

4、 Handle carefully with chips of glass that may cause injury, when the glass is broken.

9.5 Absolute Maximum Ratings and Power Protection Circuit

1、Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

2、 Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

3、 It's recommended employing protection circuit for power supply.

11.6 Operation

1、Do not touch, push or rub the polarizer with anything harder than HB pencil lead.Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

2、 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

3、Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

4、When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

9.7 Static Electricity

1、Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

2、 Because LCD module uses CMOS-IC on TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge.

3、Persons who handle the module should be grounded through adequate methods.

9.8 Disposal

When disposing LCD module, obey the local environmental regulations.

9.9 OTHERS

1、A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight land strong UV rays.

2、 Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.

3、 For the packaging box, please pay attention to the followings:

4、Packaging box and inner case for LCD are designed to protect the LCDs from the damage or scratching during transportation. Please do not open except picking LCDs up from the box.

5、 Please do not pile them up more than 6 boxes. (They are not designed so.) And please do not turn over.

6、 Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.

7、Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)

10.0 Packing form-TBD

LEADTEK DISPLAY

深圳市丽台电子有限公司

Shenzhen Leadtek Electronics Co.,Ltd

Quality inspection standards

品质允收标准

MODEL No. / 产品型号： **Applies 10 inches or more TFT-LCD Panel**
UPDATED DATE / 生效日期： **2022-05-20**
VERSION / 版 本： **A0**
Customer Signature/客户签字： _____

RECORD OF REVISION/修订履历：

Version 版本	Revision Record 修订内容	Compile 修订者	Date of Revision 修订日期
V0	首发/Starting	Green	2022.05.20

1.Scope 1适用范围

This document shall be applied to 10 inches or more TFT-LCD Panel.

本文件适用于10 寸及以上 TFT-LCD Panel.

2.Inspection and Environment onditions/检查条件与环境

2. 1 Inspection Conditions 检查条件:

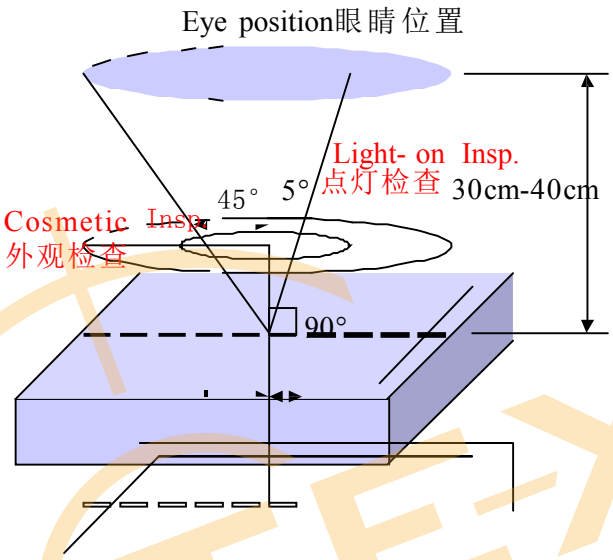
(1) Inspection Distance检测距离: 35 cm±5cm

(2) Each picture /每个画面：2~3 secs/秒，Cosmetic Inspection/外观10~12 secs/秒

(3) View Angle观看角度:

Light-on Inspection Angle点灯检验角度 ： ±45°

Cosmetic Inspection Angle外观检验角度 ： ±45°



(Perpendicular to LCD panel surface垂直于液晶显示表面)

2.2 Environment Conditions环境条件:

Ambient Temperature 温度		25℃±5℃
Ambient Humidity 湿度		55±5%RH
Ambient Illumination 亮度	Cosmetic Inspection 外观检验	800-1000 Lux
	Functional Inspection 点灯检验	200~300Lux

2.3 Sampling Conditions 抽样条件:

(1) Lot Size ： Quantity of shipment lot per model/.

批量：单次运送单一机型数量

(2) Sampling Method ：
抽样方法：

Sampling Plan 抽样计划		GB2828/2003
		Normal Inspection, Single Sampling 正常检验、单次抽样
		Geneal II Inspection 普通二级
AQL	Major Defect 主要缺点	0.25
	Minor Defect 次要缺点	0.65

(3) The classification of Major(MA) and Minor(MI) defects is shown as 3. Inspection Criteria.
主缺(MA)及次缺(MI)定义于"3.检查标准"

3.Terms and Definitions/术语和定义

3.1 Classification of defects缺陷的分类:

Major defects: A major defect is a defect that is likely to result in failure, or to reduce materially the usability of the product for its intended purpose.

主要缺陷：会导致产品功能失效或减少产品可用性的缺陷。

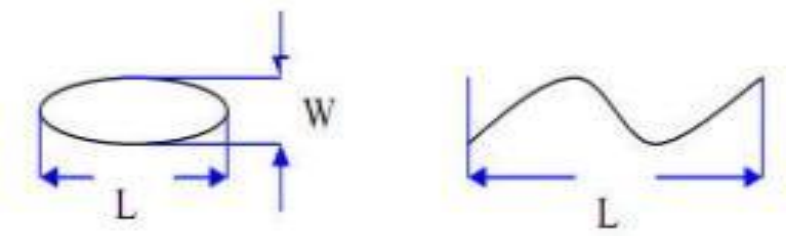
Minor defects: A minor defect either is a defect that is not likely to reduce materially the usability of the product for its intended purpose, or is a departure from an established having little bearing on the effective use or operation of the product.

次要缺陷：不会导致产品功能失效，不会减少产品的有效使用和操作。

3.2 Extraneous substances that can be wiped out ,like Finger point,Particles are not cnsidered as a defect . 可以被擦拭干净的表面物质不视为缺陷 (如手指印，尘粒) 。

3.3 Defects on the Black Matraix(outside ofActive Area) are not considered as a defect . BM 区域 (AA 区以外) 的缺陷不视为缺陷。

3.4 Size of circular defect,is defined by diameter"D" 。The defect average diameter D=1/2(W+L) 圆形缺陷的大小是由直径 D 定义的。缺陷的平均直径 D=1/2(W+L)



3.5 When defect size L≥2W,the defect count as liner type defect.Size of linear defect is defined by length(L) and the maximum width(W).

当缺陷尺寸 L≥2W 时，被视为线状缺陷。线状缺陷是由长度 (L) 和最大宽度 (W) 定义的。 3.6 3.6 Mura criteria :judged by ND filter6%,and can't be seen under at ND filter 6% .

3.6 MURA 判断标准：使用 ND6%判定，且透过 ND6% ，遮住不可见.

3.7 Dot defect is defind as the defective area of the dot is larger than 50% of the dot area and is visible through 6% ND filter

DOT 定义为点缺陷面积大于 50% DOT 面积, 且透过 ND6%遮住是可见的.

The drawing of 1/2 area sub-pixel definition: The 1/2 area sub-pixel can be defined as below one or more of specific shapes

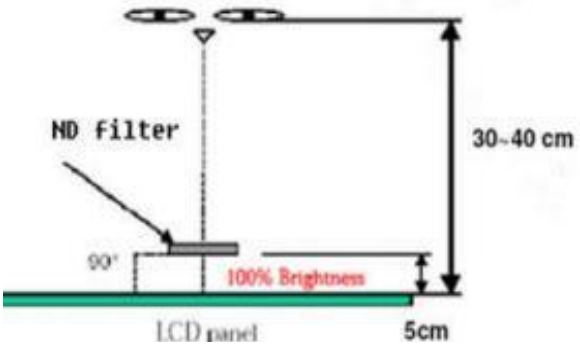
1/2 面积的子像素定义绘图：1 / 2 面积的子像素可以定义为如下一个或多个特定形状图：

3.8 A dot defect that is smaller than the defined dot defect will be treated as small bright dot. 细碎亮点：小于"DOT 定义"的点缺陷视为细碎亮点。

I 区与 O 区比例：1：2：1

3.9 Inspection method of ND Filter - holding ND filter in front of the panel around 5cm and examine the panel from 35±5 cm in the front view for 2~3 second.

ND 卡的检查方法：在面板上方大约 5CM 处握住 ND 卡，眼睛距离面板 30-40CM ，通过 2~3 秒观察。



4. Inspection Criteria 检验标准

4.1 Appearance Inspection specification 外观检查规格:

Judge area 区域	Judge item 项目	Specification inspection 检查规格	Judge criterion	
			Major	Minor
Silicone 硅胶	Silicone spread 硅胶涂布	The height can't over C/F , color filter , or gomu 高度不能过超 C/F		MI
	Silicone residue 硅胶残余	Can't cover polarizer, FPC …etc. 不能覆盖 POL, FPC 等		MI
LCD 玻璃	Wire(on Array) 线路	No damage 不能损伤	MA	
	Edge 边缘	No extended crack 不可有延伸性裂纹	MA	
PCBA Connector FPC/FFC	Appearance 外观	Scratch or damage result in copper expose is not allowed 划伤或损伤不允许导致出现露铜		MI
	Component 零件	No damage 不能损伤	MA	
	Connection status 连接状况	Need correct connection 需要正确连接	MA	
	Broken 破裂	Not allowable 不允许	MA	
	Folding sign 对位记号折叠	Not allowable 不允许	MA	
POL 偏光片	Scract on the polarizer 偏光片划伤	1.W≤0.10mm; L≤5mm, Ignore (忽略)		MI
		2.0.10mm<W≦0.20mm ; L≤5mm ; N≤4 ; DS≥10mm		
		3.0. 20mm＜W; 5mm＜ L , Not allowable不允许		

Judge area 区域	Judge item 项目	Specification inspection 检查规格	Judge criterion	
			Major	Minor
POL 偏光片	Dent on the polarizer 偏光片凹痕	1.D＜0. 30mm，Ignore（忽略）		MI
		2.0.30mm＜D≤0.50mm；N≤4；DS≥10mm		
		3.0.50mm＜D，Not allowable不允许		
	POL Linear bubble 线状气泡	1.W≤0.10mm；L≤5mm，Ignore（忽略）		MI
		2.0.10mm<W≦0.20mm ; L≤5mm ; N≤4 ; DS≥10mm		
		3.0. 20mm＜W；5mm＜ L，Not allowable不允许		
	POL dot bubble 点状气泡	1.D＜0. 30mm，Ignore（忽略）		MI
		2.0.30mm＜D≤0.50mm；N≤4；DS≥10mm		
		3.0.50mm＜D，Not allowable不允许		
	POL edge bubble 片边缘气泡	1. The display area is 1/2BM outside，Not allowable 显示区往外 1/2BM 区域内，不允许 2. The display area is outside the outer 1/2BM area，Not allowable 显示区往外1/2BM区域以外，不管控		MI

Judge area 区域	Judge item 项目	Specification inspection 检查规格	Judge criterion	
			Major	Minor
TP&CG	Foreign Material in spot shape 点状异物	1.D≤0.30mm；Ignored（忽略） 2.0.30mm＜D≤0.50mm；N≤4；DS≥10mm 3.D＞0.50mm；Not allowable不允许		MI
	Fisheye/bubbles 鱼眼/气泡	1.D≤0.30mm；Ignored（忽略） 2.0.30mm＜D≤0.50mm；N≤4；DS≥10mm 3.D＞0.50mm；Not allowable不允许		MI
	Scratches on the surface 表面划伤	1.W≤0.10mm；Ignored（忽略） 2.0.10mm<W≤0.20mm，L≤5mm；N≤4；DS≥10mm 3.W＞0.20mm，L＞5mm；Not allowable不允许		MI
	Collapse corner、Crash edge 崩角、崩边	Product front:/产品正面： collapse corners, collapsed edges are not allowed 崩角、崩边不允许； Product back/产品背面： X≤ 0.5 , Y≤0.5，Z≤1/2T；N≤4；DS≥10mm	MA	
	Printed fonts/LOGO 丝印/LOGO	Printed fonts/LOGO clarity、complete、content right 字体/LOGO丝印清晰、完整、内容正确		MI
	Broken 破损	Not allowable不允许	MA	
	Dirty surfaces 表面脏污	Dirt cannot be wiped， Not allowable 不可擦拭的脏污，不允许		MI
	IR hole IR孔	Black spots/黑点： W ≤0.15mm，N≤2，Not visible against a black background/黑色背景下不可见		MI
		IR hole Scratches： 1.W＜0.05mm，Ignored（忽略） （Dense points Not allowable 不允许密集）； 2.0.05mm＜W≤0.07mm；L≤2mm；N≤2； 3.W＞0.07mm，L＞2mm，Not allowable 不允许		MI

4.2 Electrical Inspection specification电性检查规格:

Item 项目	Judgment Criteria 判定标准	Judge criterion	
		Major	Minor
LCD Bright /Dark dot 玻璃亮点/暗点	1.D≦0. 30mm， Ignored（忽略），Not dense（不可密集） 2.0.30mm<D≦0.50mm ； N≦4 ； DS≥10mm 3.D＞0.50mm ，Not allowed/不允许		MI
Mura	Invisible through 6% ND filter，200~300Lux 透过ND6% 遮住 ， 目测不可见即为OK， 200~300Lux		MI
Small bright dot 细碎亮点	Not allowed if it can be observed through ND Filter6% 透过ND6%目测看得见，不允许		MI
ZBD Rate 玻璃亮点比率	90:10		MI
Light Leakage 漏光	Invisible through 6% ND filter，OK 透过ND6%遮住目测不可见即为OK If necessary,set up set up Limit Sample. 如果有必要，可制订限度样品		MI
Bubble in Cell (LC Bubble/Actice Area) CELL气泡 (AA区LCD气泡)	Eyes should not find it . 目视观察不可见，视为 OK	MA	

Item 项目	Judgment Criteria 判定标准	Judge criterion	
		Major	Minor
Foreign Material in spot shape 点状异物	1.D≦0.30mm， Ignored（忽略） 2.0.30mm<D≦0.50mm ； N≦4； DS≥10mm 3.D＞0.50mm ， Not allowable/不允许		MI
Foreign Material in line or spiral shape 线状异物	1.W≦0.10mm ， Ignored（忽略） 2. 0.10mm<W≦0.20mm ； L≤5mm ； N≦4 3.W＞0.20mm ； L＞5mm ， Not allowable/不允许		MI
White dot in back-light 白点	1.D≦0. 30mm，Ignored（忽略） 2.0.30mm<D≦0.50mm ； N≦4 ； DS≥10mm 3.D＞0.50mm ， Not allowed/不允许		MI
TP no touch 无触摸	Not allowable 不允许	MA	
Abnormal Disply 显示异常	Not Allowed 不允许	MA	
NO display 无显示	Not Allowed 不允许	MA	
Line Defect 缺线	Not Allowed 不允许	MA	
Angle of view error 视角错误	Not Allowed 不允许	MA	
Tect crostalk 不消失的残影	Not Allowed 不允许	MA	

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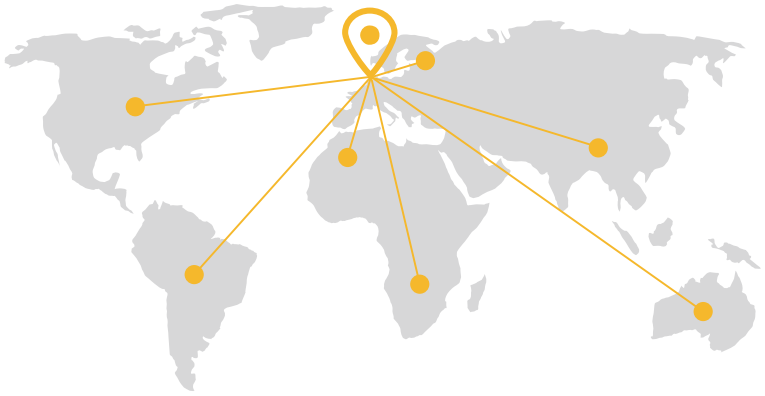

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