13.3 inch
E-paper Display Series

WAA1330A2BNC3NXXX000

Product Specifications

Customer	**Standard**
Description	**13.3" E-PAPER DISPLAY**
Model Name	**WAA1330A2BNC3NXXX000**
Date	**2025/02/18**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**

CONTENTS

1. Over View

WAA1330A2BNC3NXXX000 is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The display is capable to display image at 1-bit white, black and red full display capabilities. The 13.3inch active area contains 960×680 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

◆960×680 pixels display

◆High contrast High reflectance

◆Ultra wide viewing angle Ultra low power consumption

◆Pure reflective mode

◆Bi-stable display

◆Commercial temperature range

◆Landscape portrait modes

◆Hard-coat antiglare display surface

◆Ultra Low current deep sleep mode

◆On chip display RAM

◆Built-in temperatur sensor

◆Waveform can stored in On-chip OTP or written by MCU

◆Serial peripheral interface available

◆On-chip oscillator

◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage

◆I^2C signal master interface to read external temperature sensor

3. Mechanical Specification

Parameter	Specifications	Unit	Remark
Screen Size	13.3	Inch	
Display Resolution	960(H)×680(V)	Pixel	DPI:88
Active Area	275.52×195.16	mm	
Pixel Pitch	0.287×0.287	mm	
Pixel Configuration	Rectangle		
Outline Dimension	286.32(H)×212.26 (V) ×1.20(D)	mm	
Weight	106.7±0.5	g	

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
KS	Black State L* value		-	13	15		3-1
	Black State A* value		-	4	6		3-1
	Black Ghosting ΔE		-	2	-		3-1
	After 24 hour colour changed		-	2	-		3-4
WS	White State L* value		62	65	-		3-1
	White State A* value		-	0	1		3-1
	White Ghosting ΔE		-	2	-		3-1
	After 24 hour colour changed		-	2	-		3-4
RS	Red State L* value		27	28	32		3-1
	Red State A* value		36	40	45		3-1
	Red Ghosting ΔE		-	3	-		3-1
	After 24 hour colour changed		-	2	-		3-4
T update	Image update time	at 23 °C	-	17	-	sec	
R	White Reflectivity	White	30	34	-	%	3-1
CR	Contrast Ratio	Indoor	15:1	20:1	-		3-1 3-2
GN	2Grey Level	-	-	-	-		
Life		Temp:23±3°C Humidity:55±10%RH		5years			3-3

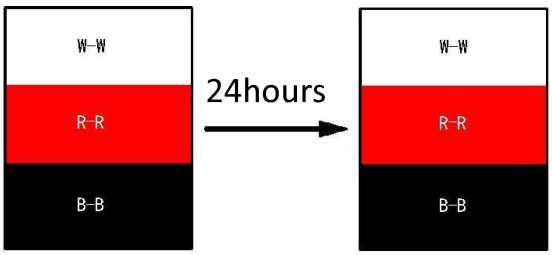
Notes:

3-1. Luminance meter: Eye-One Pro Spectrophotometer.

3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3. When the product is stored. The display screen should be kept white and face up.

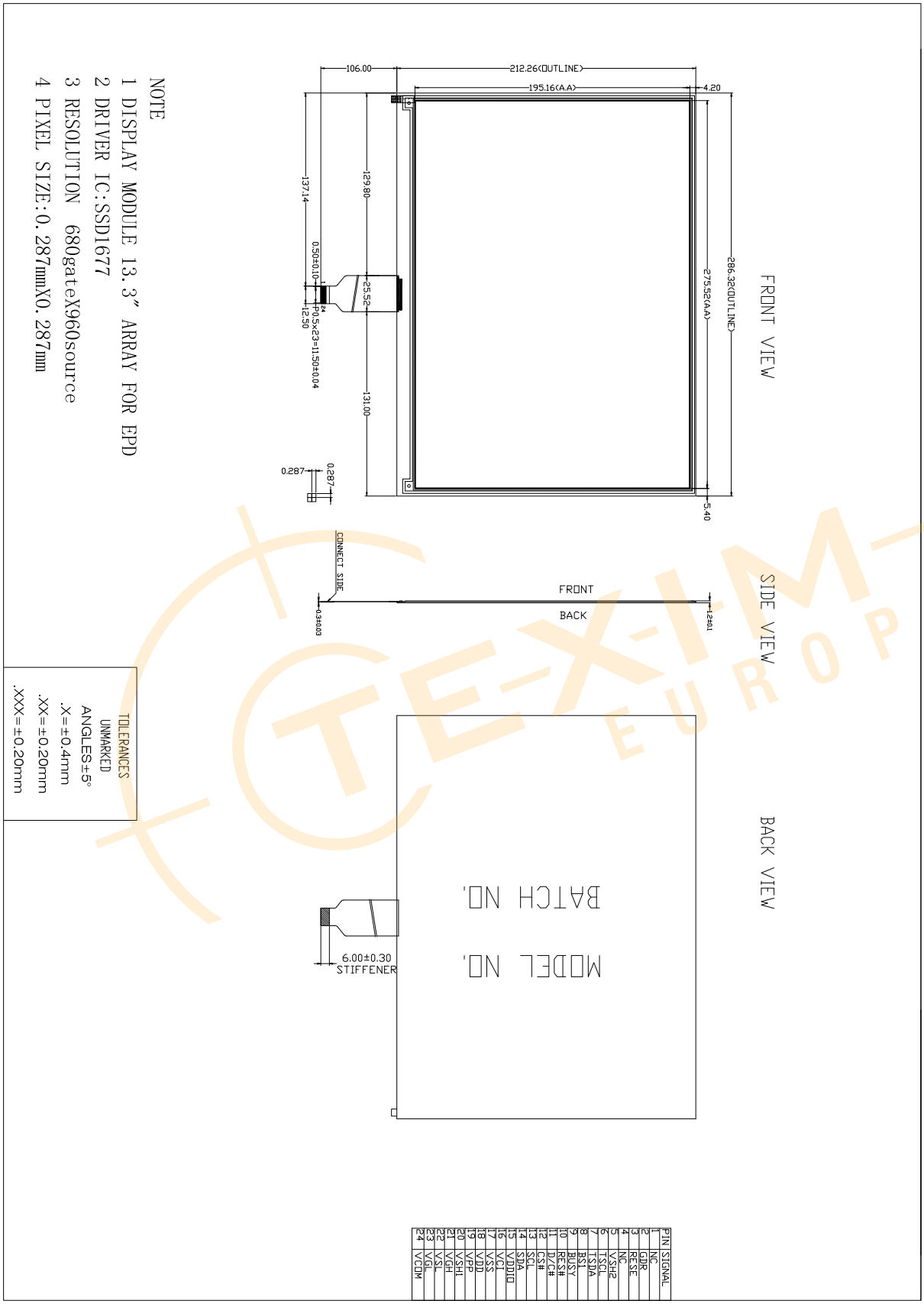
3-4. After 24hours Colour Changed:



W:MaxΔE(W-W)<2, K:MaxΔE(B-B)<2, R: MaxΔE(Y-Y)<2.

L: black and white luminance value, A: red luminance value, ΔE: color difference

4.Mechanical Drawing of EPD Module



5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin,I /O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor.

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +40	ºC.
Storage Temp range	TSTG	-25 to+70	ºC.
Optimal Storage Temp	TSTGo	23±3	ºC.
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

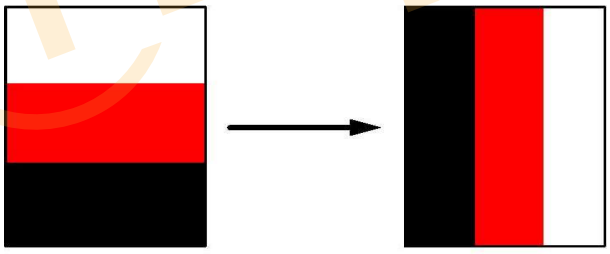
1. Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
2. We guarantee the single pixel display quality for 0-35℃, but we only guarantee the barcode readable for 35-40℃.
3. The storage time is within 10 days for -25℃ ~ 0℃ or 40℃ ~ 60℃. The display screen should be kept white and face up.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.2	3.0	3.3	V
Core logic voltage	V_{DD}		VDD	1.7	1.8	1.9	V
High level input voltage	V_{IH}	-	-	0.8 V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{CI}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{CI}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{CI}	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	75	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_VCI	V_{CI} =3.0V	-	-	25	-	mA
Image update time	-	23 ºC	-	-	22	-	sec
Typical peak current	Iopr_VCI	2.2V~3.7V			100	200	mA
Sleep mode current	Islp_V_{CI}	DC/DC off No clock No input load Ram data retain	-	-	20	-	uA
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data not retain	-	-	3	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 3 scale pattern to vertical 3 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by WINSTAR Display .
4. Electrical measurement: Tektronix oscilloscope - MDO3024, Tektronix current probe–TCP0030A.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-	TBD	-	V
Positive Source output voltage	V_{SH}	-	S_0~S_{959}	+14.8	+15	+15.2	V
Negative Source output voltage	V_{SL}	-	S_0~S_{959}	-15.2	-15	-14.8	V
Positive gate output voltage	Vgh	-	G_0~G_{679}	+19.5	+20	+20.5	V
Negative gate output voltage	Vgl	-	G_0~G_{679}	-20.5	-20	-19.5	V

Note: VGH,VGL,VSH,VSL drop voltage <2V.

6.4 MCU Interface

6.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

6.4.2 MCU Serial Interface (4-wire SPI)

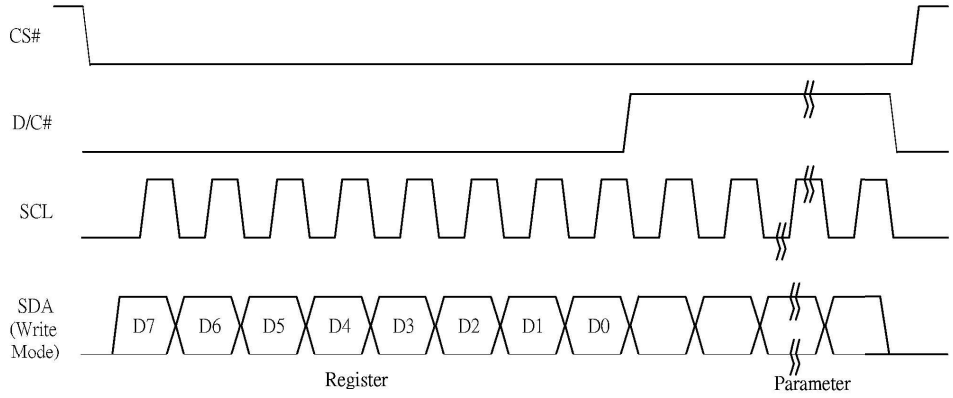
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte . The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

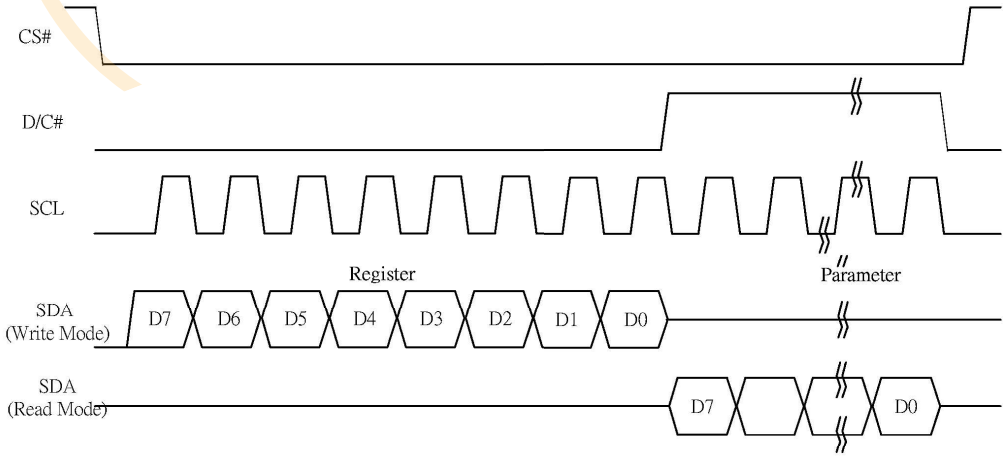
Figure 6-1: Write procedure in 4-wire SPI mode



In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-2: Read procedure in 4-wire SPI mode



6.4.3 MCU Serial Interface (3-wire SPI)

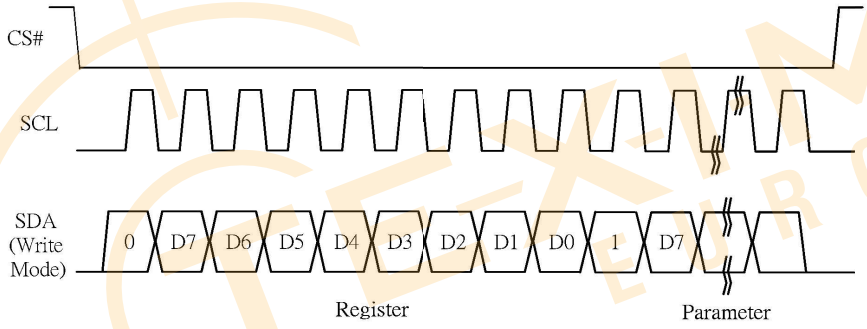
The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

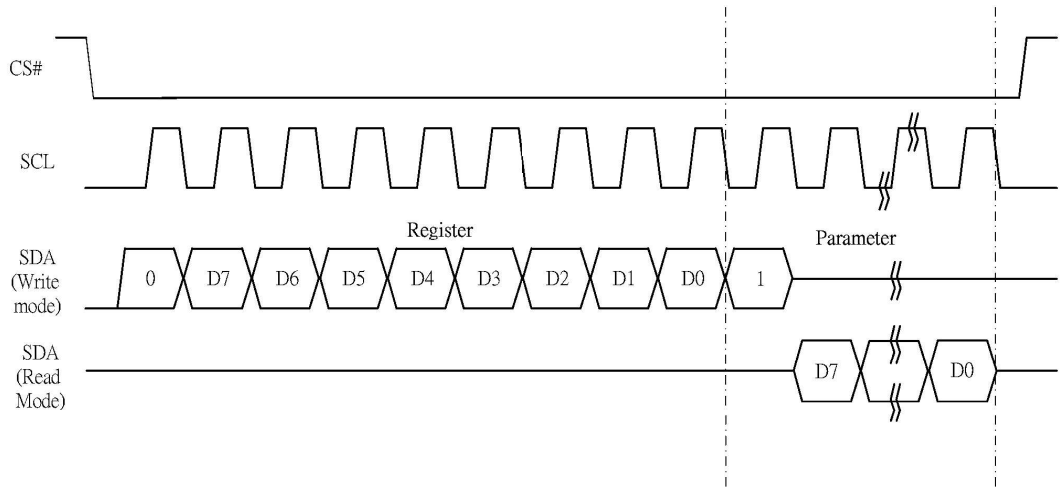
Figure 6-3: Write procedure in 3-wire SPI mode



In the Read mode:

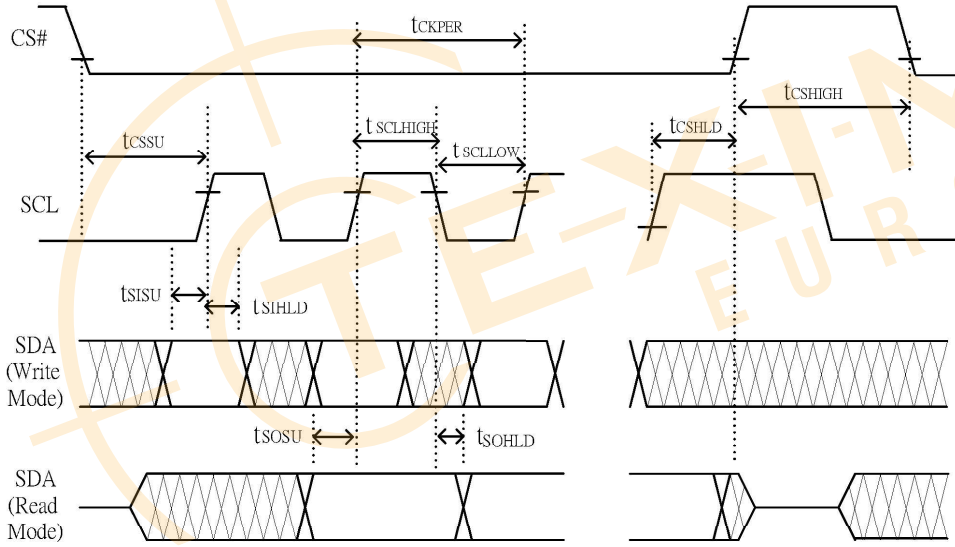
1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode



6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.



Changed Diagram

Serial Interface Timing Characteristics

(VCI - VSS = 2.2V to 3.7V, TOPR = 23°C, CL=20pF)

Write mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	60			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	65			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

7.Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output control</td><td rowspan="4">Gate setting
Set A[9:0]=2A7h[POR] ,680MUX
Set B[2:0]=000[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A9</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Gate Driving voltage control</td><td rowspan="2">SetGate Driving voltage
A[4:0]=17h[POR],VGH at 20V[POR]
VGH setting from 12V to 20V</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>04</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Source Driving voltage control</td><td rowspan="4">SetSource Driving voltage
A[7:0]= 41h[POR],VSH1 at 15V
B[7:0]=A8h[POR],VSH2 at 5.0V
C[7:0]= 32h[POR], VSL at -15V</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td><td>C0</td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Deep Sleep mode</td><td rowspan="2">Deep Sleep mode Control
<table><tr><td>A[1:0] :</td><td>Description</td></tr><tr><td>00</td><td>Normal Mode [POR]</td></tr><tr><td>11</td><td>Enter Deep Sleep Mode</td></tr></table>After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>11</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Data Entry mode setting</td><td rowspan="2">Define data entry sequence
A [1:0] = ID[1:0]Address automatic increment / decrement setting
The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.
00 –Y decrement, X decrement,
01 –Y decrement, X increment,
10 –Y increment, X decrement,
11 –Y increment, X increment [POR]
A[2] = AM
Set the direction in which the address counter is updated automatically after data are written to the RAM.
AM= 0, the address counter is updated in the X direction. [POR]
AM = 1, the address counter is updated in the Y direction.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>SWRESET</td><td>It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode
During operation ,BUSY pad will output high.
Note: RAM are unaffected by this command.</td></tr>
</table>

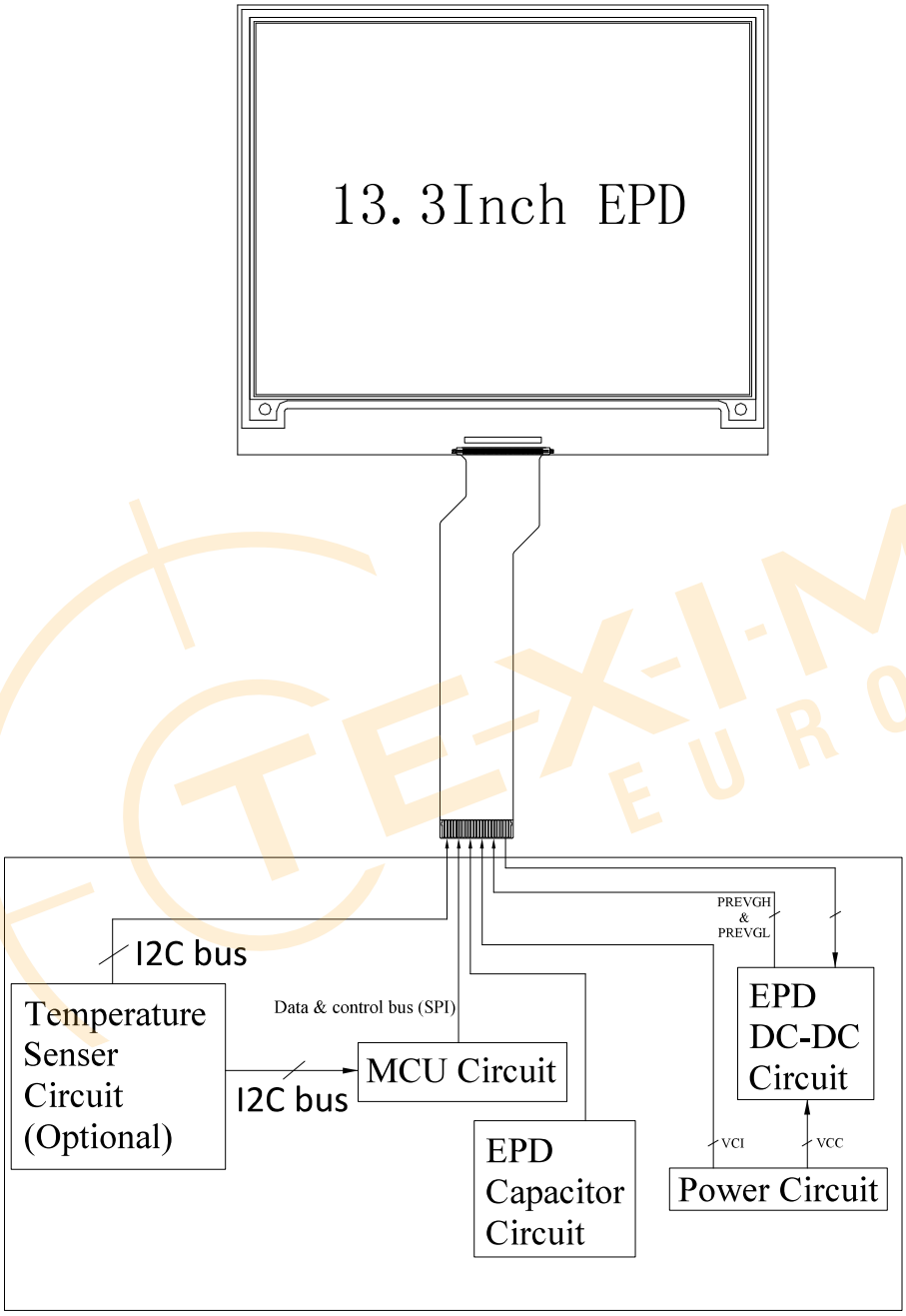
<table>
<tr><td>0</td><td>0</td><td>18</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Temperature Sensor Control</td><td rowspan="2">Temperature Sensor Selection
A[7:0] = 48h [POR], external temperature sensor
A[7:0] = 80h Internal temperature sensor</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>1A</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="3">Temperature Sensor Control (Write to temperature register)</td><td rowspan="3">Write to temperature register.
A[11:0]=7FFh[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A11</td><td>A10</td><td>A9</td><td>A8</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence
The Display Update Sequence Option is located at R22h
User should not interrupt this operation to avoid corruption of panel images.</td></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Display Update Control 1</td><td rowspan="2">RAM content option for Display Update
A[7:0]=00h[POR]
A[7:4] Red RAM option
0000 Normal
0100 Bypass RAM content as 0
1000 Inverse RAM content

A[3:0] BW RAM option
0000 Normal
0100 Bypass RAM content as 0
1000 Inverse RAM content</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:
Enable the stage for Master Activation
Setting for LUT from MCU
Enable Clock Signal,
Then Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC
C7
Setting for LUT from OTP according to external Temperature Sensor operation
Then Enable Analog
Then Load LUT
90
Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC
47</td></tr>
<tr><td></td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM (BW)</td><td>After this command, data entries will be written into the 1RAM until another command is written. Address pointers will advance accordingly.
For Write pixel:
Content of write RAM(BW)=1
For Black pixel:
Content of write RAM(BW)=0</td></tr>
</table>

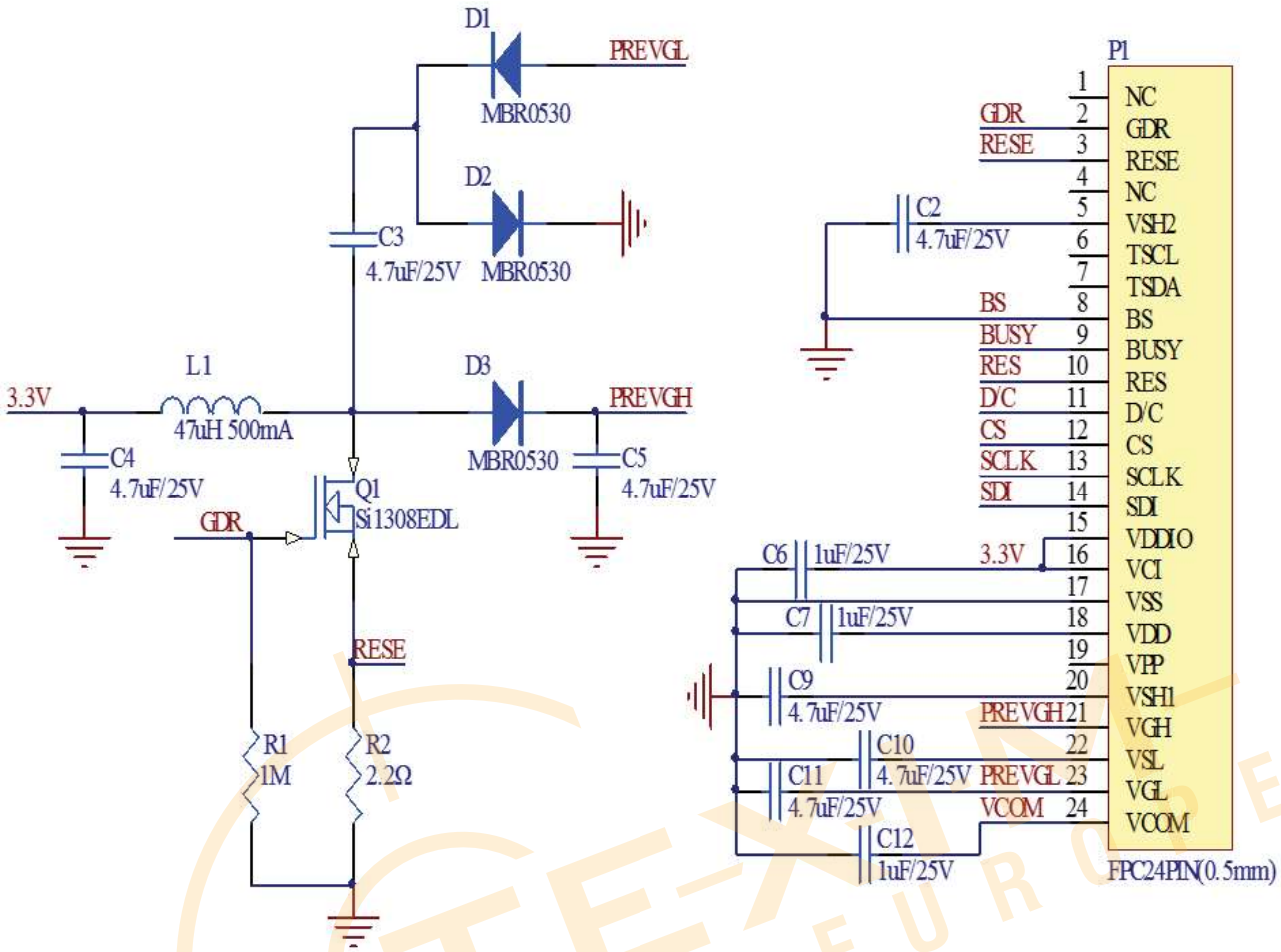
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the 2 RAM until another command is written. Address pointers will advance accordingly. For RED pixel: Content of write RAM(RED)=1 For White/Black pixel: Content of write RAM(RED)=0
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Set A[7:0]=50h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read	Read Register stored in OTP: 1. A[7:0]~ B[7:0]: VCOM Information 2. C[7:0]~G[7:0]:Display mode 3. H[7:0]~K[7:0]: Waveform Version [4bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
1	1		K7	K6	K5	K4	K3	K2	K1	K0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x21] A[5]: HV Ready Detection flag [POR=1] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A5	A4	0	0	A1	A0		
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [105 bytes].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		

<table>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Border Waveform Control</td><td rowspan="2">Select border waveform for VBD
A [7:0]=C0h[POR],set VBD as HIZ
A [7:6] Select VBD option<table><tr><td>A[7:6]</td><td>Select VBD as</td></tr><tr><td>00</td><td>GS Transition
Define A[1:0]</td></tr><tr><td>01</td><td>Fix Level
Define A [5:4]</td></tr><tr><td>10</td><td>VCOM</td></tr><tr><td>11[POR]</td><td>HIZ</td></tr></table>A [5:4] Fix Level Setting for VBD<table><tr><td>A[5:4]</td><td>VBD level</td></tr><tr><td>00[POR]</td><td>VSS</td></tr><tr><td>01</td><td>VSH1</td></tr><tr><td>10</td><td>VSL</td></tr><tr><td>11</td><td>VSH2</td></tr></table>A[1:0]) BW Transition setting for VBD<table><tr><td>A[1:0]</td><td>VBD Transition</td></tr><tr><td>00 [POR]</td><td>LUT0</td></tr><tr><td>01</td><td>LUT1</td></tr><tr><td>10</td><td>LUT2</td></tr><tr><td>11</td><td>LUT3</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>44</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Set RAM X - address Start / End position</td><td rowspan="4">Specify the start/end positions of the window address in the X direction by an address unit
A[9:0]: XSA[9:0], X Start, POR = 000h
B[9:0]: XEA[9:0], X End, POR = 3BFh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A_9</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>B_9</td><td>B_8</td></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="4">Set Ram Y-address Start / End position</td><td rowspan="4">Specify the start/end positions of the window address in the Y direction by an address unit
A[9:0]: YSA[9:0], Y Start, POR = 000h
B[9:0]: YEA[9:0], Y End, POR = 2A7h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A_9</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>B_9</td><td>B_8</td></tr>
<tr><td>0</td><td>0</td><td>4E</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td rowspan="3">Set RAM X address counter</td><td rowspan="3">Make initial settings for the RAM X address in the address counter (AC)
A[9:0]: 000h[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A_9</td><td>A_8</td></tr>
<tr><td>0</td><td>0</td><td>4F</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td rowspan="4">Set RAM Y address counter</td><td rowspan="4">Make initial settings for the RAM Y address in the address counter (AC)
A[9:0]: 000h[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A_9</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
</table>

8. Block Diagram



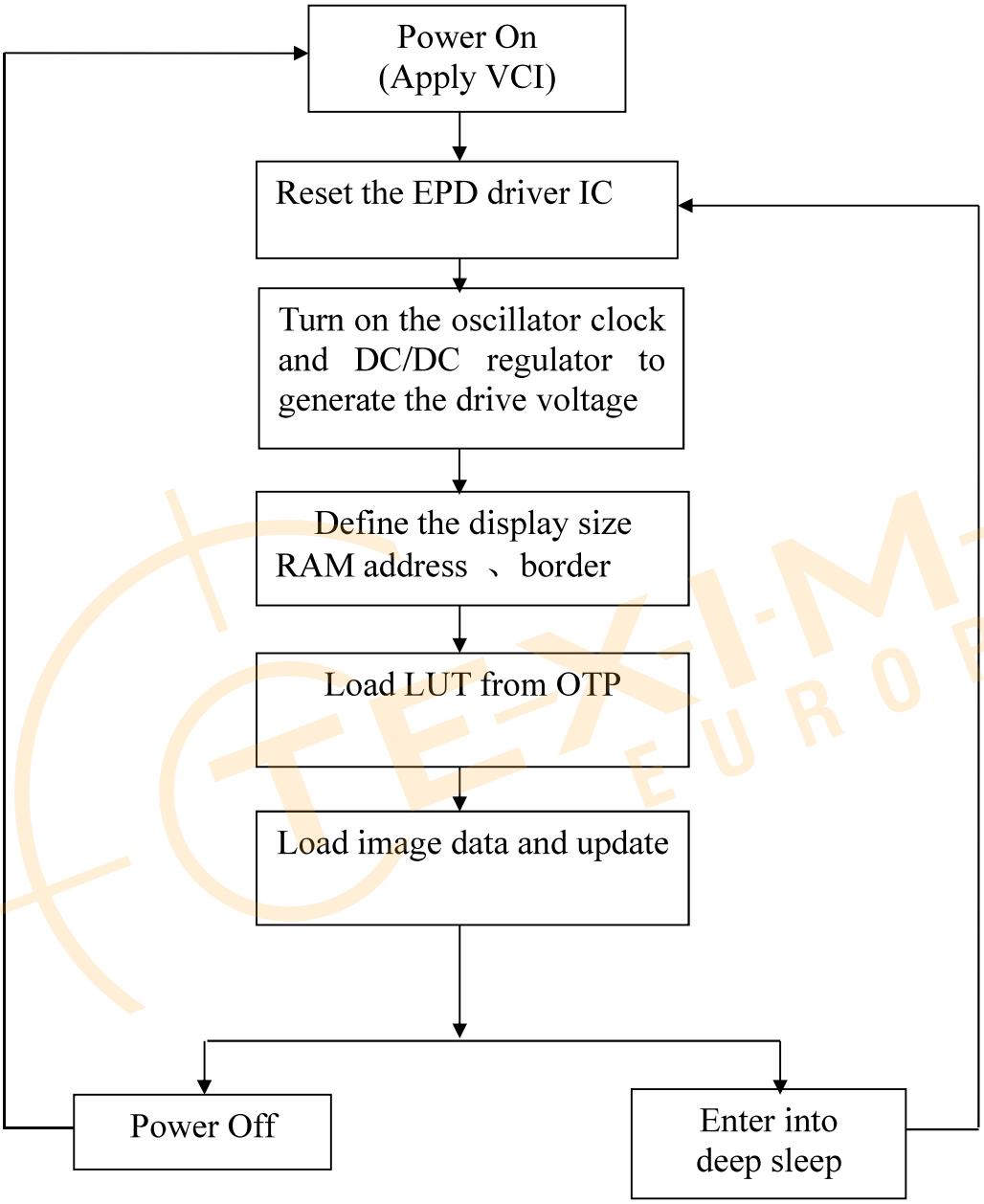
9. Typical Application Circuit with SPI Interface



Part Name	Requirements for spare part
C1—C12	0603/0805; X5R/X7R;Voltage Rating:≥25V
R1、R2	0603/0805;1% variation,≥0.05W
D1—D3	MBR0530: 1)Reverse DC Voltage≥30V 2)Io≥500mA 3)Forward voltage ≤430mV
Q1	Si1308EDL:1)Drain-Source breakdown voltage≥30V 2)Vgs(th)≤1.5V 3)Rds(on)≤400mΩ
L1	refer to NR3015: Io=500mA(max)
P1	24pins,0.5mm pitch

10 Typical Operating Sequence

10.1 LUT from OTP Operation Flow



10.2 OTP Operation Reference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RES#	low	Hardware reset
delay	200us	
RES#	high	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
Command 0x0C	Data 0xAE 0xC7 0xC3 0xC0 0x80	Booster Soft-start Control
Command 0x01	Data 0xA7 0x02 0x00	Set display size and driver output control
Command 0x11	Data 0x01	Ram data entry mode
Command 0x44	Data 0x00 0x00 0xBF 0x03	Set Ram X address
Command 0x45	Data 0xA7 0x02 0x000x00	Set Ram Y address
Command 0x3C	Data 0x01	Set border
LOAD LUT		
Command 0x18	Data 0x80	Set built-in temperature sensor
Command 0x22	Data 0xB1	Load LUT
Command 0x20		
Read busy pin		Wait for busy low
LOAD IMAGE AND UPDATE		
Command 0x4E	Data 0x00 0x00	Set Ram X address counter
Command 0x4F	Data 0xA7 0x02	Set Ram Y address counter
Command 0x24	81600 bytes	Load BW image (960/8*680)
Command 0x4E	Data 0x00 0x00	Set Ram X address counter
Command 0x4F	Data 0xA7 0x02	Set Ram Y address counter
Command 0x26	81600 bytes	Load RED image (960/8*680)
Command 0x22	Data 0xC7	Image update
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

11. Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60ºC，RH=35%，240h Test in white pattern
3	High-Temperature Operation	T=40ºC，RH=35%，240h
4	Low-Temperature Operation	0ºC，240h
5	High-Temperature, High-Humidity Operation	T=40ºC，RH=80%，240h
6	High Temperature, High Humidity Storage	T=50ºC，RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern
8	ESD Gun	Air+/-4KV;Contact+/-2KV (Naked EPD display,including IC and FPC area)

Note1： Stay white pattern for storage and non-operstion test.
Note2： Operation is black→white→red pattern, the interval is 150s.
Note3： Put in 20℃--25℃ for 1hour after test finished, The function ,appearance and display performance is ok.

12. Quality Assurance

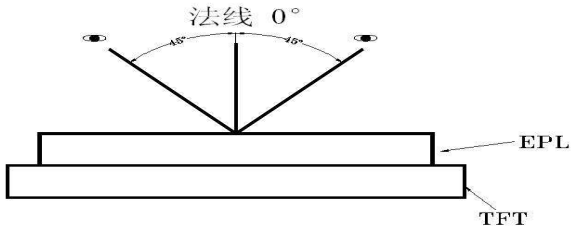
12.1 Environment

Temperature： 23±3℃, Humidity： 55±10%RH

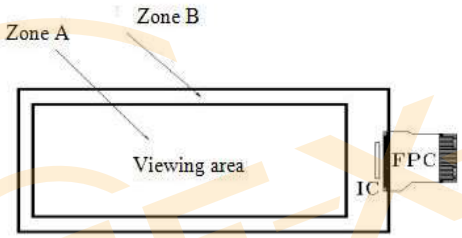
12.2 Illuminance

Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 45°surround.

12.3 Inspect method

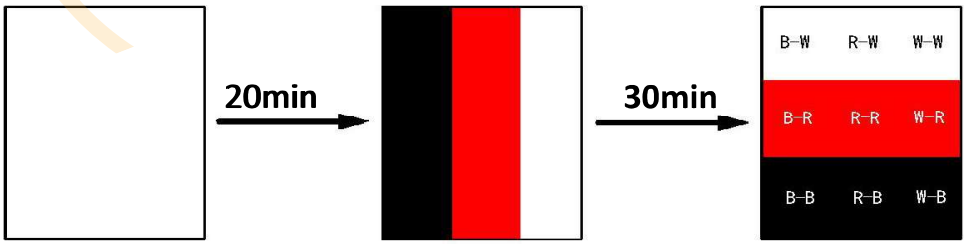


12.4 Display area



12.5 Ghosting test method

Three-color ghosting is measured with following transition from horizontal 3 scale pattern to vertical 3 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by WINSTAR Display.



1)Measurement Instruments：X-rite i1Pro

2)Ghosting formula:

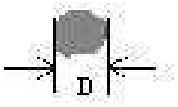
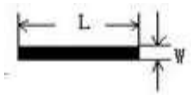
W ghosting：△E= Max (ΔEab(W-W, R-W),ΔEab(W-W, B-W),ΔEab(B-W, R-W))

K ghosting：△E= Max (ΔEab(B-B, W-B),ΔEab(B-B, R-B),ΔEab(R-B, W-B))

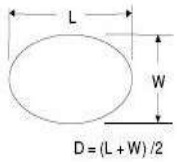
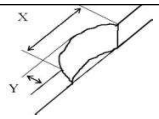
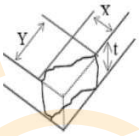
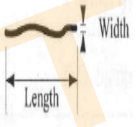
R ghosting：△E= Max (ΔEab(R-R, W-R),ΔEab(R-R, B-R),ΔEab(B-R, W-R))

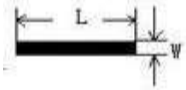
12.6 Inspection standard

12.6.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA	Visual inspection Visual/ Inspection card	Zone A
2	Black/White spots	 D≤0.4mm，Allowed 0.4mm＜D≤0.7mm。N≤6， 0.7mm＜D Not Allow	MI		
3	Black/White line (No switch)	 L≤2.0mm,W≤0.2mm negligible 2.0mm＜L≤8.0mm 0.2mm＜W≤0.5mm N≤5 allowable L＞8.0mm ,W＞0.5mm is not allowed			
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.25mm negligible 0.25mm＜D≤0.4mm N≤4 allowable D＞0.4mm is not allowed	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm And without affecting the electrode is permissible  2mm≤X or 2mm≤Y Not Allow  W≤0.1mm,L≤5mm, No harm to the electrodes and N≤2 allow	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ Goldfingers oxidation/ scratch	  Not Allow	MA	Visual / Microscope	Zone B

8	B/W Line	 L≤1.0mm,W≤0.15mm negligible 1.0mm＜L≤4.0mm 0.15mm＜W≤0.5mm N≤4 allowable L＞4.0mm ,W＞0.5mm is not allowed	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge： X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	D≤0.25mm, allow 0.25mm＜D≤0.4mm ,n≤4 allow D＞0.4mm is not allowed (n≤8 items are allowed within 5 mm in diameter)	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤0.5mm。n≤5			
13	Protect film	Surface scratch but not effect protect function, Allowed		Visual Inspection	
14	Silicon glue	Thickness≤PS surface(With protect film): Full cover the IC; Shape: The width on the FPC ≤ 0.5mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
15	Warp degree (TFT substrate)	t≤1.0mm	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

13.Packaging

TBD

14. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color(black, white, red and yellow) WINSTAR Display 's E-paper Display. And it is also added the functions of USB serial port, FLASH c hip, font chip, current detection ect.
Development Kit consists of the development board and the pinboard.

Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc.

15. Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

16. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

Disclaimer

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Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time.

All operating parameters, including typical parameters, must be validated for each customer application by the customer’s technical experts.

Please contact us if you have any questions about the contents of the datasheet.

This may not be the latest version of the datasheet. Please check with us if a later version is available.

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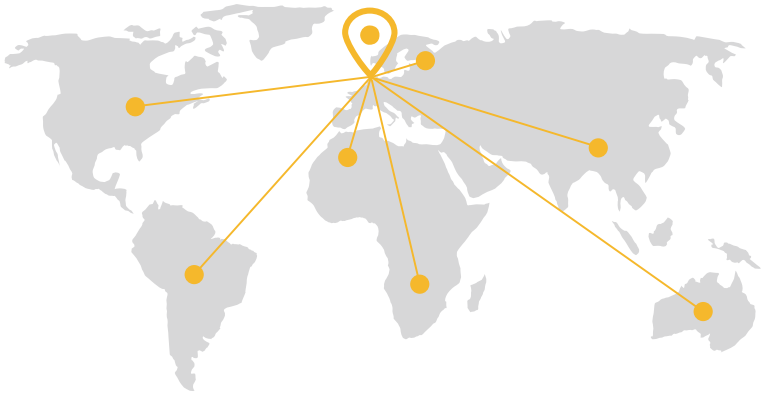

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