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2.13 inch E-paper Display Series



Customer St	tandard
Description 2.	.13" E-PAPER DISPLAY
Model Name W	AA0213A2CNA6NXXX000
Date 20	025/01/24
Revision 1.	.0

D	esign Engineerin	Ig
Approval	Check	Design



REVISION HISTORY

F	Rev	Date	Item	Page	Remark
	0	JAN.24.2025	New Creation	ALL	



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1. Over View

WAA0213A2CNA6NXXX000 is a reflective electrophoretic technology display module on an active matrix TFT substrate. The panel is capable of displaying black, white, yellow and red images depending on the associated lookup table used. The circuitry on the panel includes an integrated gate and source driver, timing controller, oscillator, DC-DC boost circuit, and memory to store the frame buffer and lookup tables, and additional circuitry to control VCOM and BORDER settings.

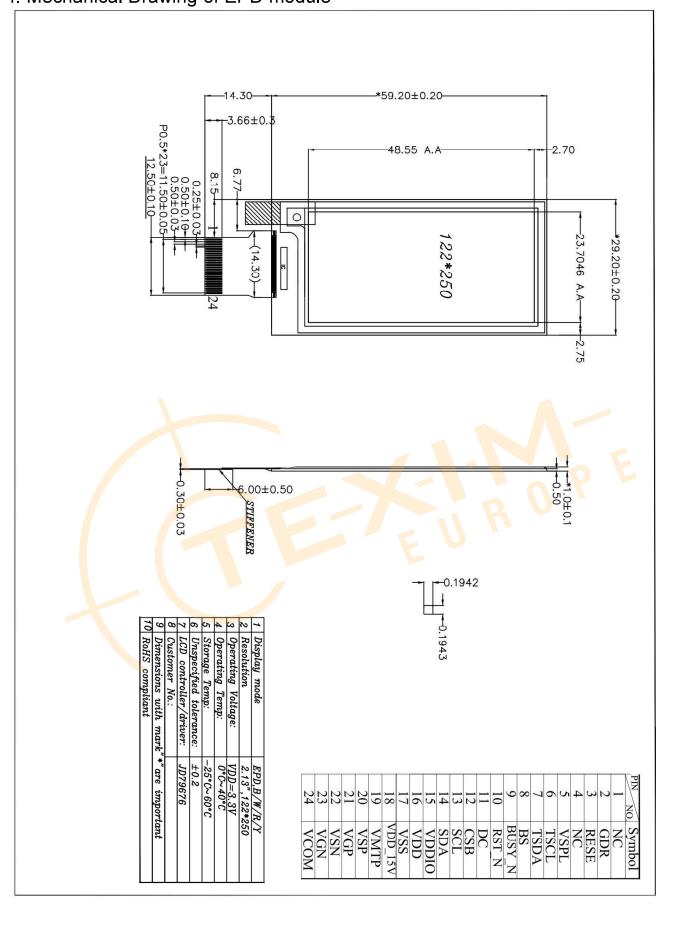
2. Features

- Highlight Red and Yellow color
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I²C signal master interface to read external temperature sensor
- Available in COG package

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	122 (H)×250 (V)	Pixel	Dpi:130
Active Area	23.7046×48.55	mm	
Pixel Pitch	0.1942×0.1943	mm	
Pixel Configuration	Rectangle		
Outline Dimension	29.2(H)×59.2(V) ×1.0(D)	mm	
Weight	3.3 ± 0.5	g	

4. Mechanical Drawing of EPD module



5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	0	This pin is N-MOS gate control.	
3	RESE	Р	Current sense input for control loop.	
4	NC		Do not connect with other NC pins	Keep Open
5	VSPL	Р	Positive source voltage	
6	TSCL	I/O	I ² C clock for external temperature sensor (I ² C interface need external pull high resistance.) Must pull high or low if not used. (Default low)	
7	TSDA	I/O	I ² C data for external temperature sensor (I ² C interface need external pull high resistance.) Must pull high or low if not used.(Default low)	
8	BS	Ι	Input interface setting.	
9	BUSY_N	0	This pin indicates the driver status.	
10	RST_N	Ι	Global reset pin. Low reset. (normal pull high)	
11	DC	Ι	Serial communication Command/Data input	
12	CSB	Ι	Serial communication chip select.	E
13	SCL	Ι	Serial communication clock input.	5
14	SDA	I/O	Serial communication data input.	
15	VDDI0	Р	IO voltage supply	
16	VDD	Р	Digital/Analog power.	
17	VSS	Р	Digital ground	
18	VDD_15V	Р	1.5V voltage input &output	
19	VMTP	Р	MTP program power	
20	VSP	Р	Positive source voltage	
21	VGP	Р	Positive gate voltage	
22	VSN	Р	Negative source voltage.	
23	VGN	Р	Negative gate voltage	
24	VCOM	0	VCOM output.	

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
	VDD,		
Logic supply voltage	AVDD,VDDIO,	-0.3 to +6.0	V
	VDD1,VPP		
Digital input voltage	VI	-0.3 to VDDIO+0.3	V
Operating Temp range	TOPR	0 to +40	° C
Storage Temp range	TSTG	-25 to +70	° C
Optimal Storage Temp	TSTGo	23±2	° C
Optimal Storage Humidity	HSTGo	55±10	%RH

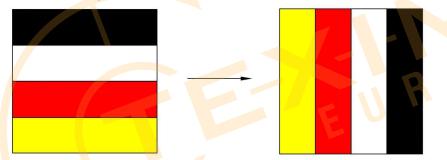
Note: Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.



Parameter	Symbol	Conditions	Applica ble pin	Min.	Тур.	Max	Units
Single ground	Vss	-		-	0	-	V
Logic supply voltage	V _{DD}	-	VDD	2.3	3.3	3.6	V
Core logic voltage	V _{IO}	-	VIO	2.3	3.3	3.6	V
High level input voltage	V _{IH}	-	-	0.7V _{IO}	-	V _{IO}	V
Low level input voltage	V _{IL}	-	-	GND	-	$0.3 V_{\text{DD}}$	V
High level output voltage	V _{OH}	IOH = 400Ma	-	V _{IO} -0.4	-	-	V
Low level output voltage	Vol	IOL = -400Ma	-	GND	-	GND +0.4	V
Typical power	$\mathbf{P}_{\mathrm{TYP}}$	$V_{DD} = 3.3 V$	-	-	10.89	13.2	mW
Deep sleep mode	PSTPY	$V_{DD} = 3.3 V$	-	-	0.003	0.0165	mW
Typical operating current	Iopr_V _{DD}	$V_{DD} = 3.3 V$	-	-	3.3	4	mA
Image update time	-	25 °C	-	-	26	-	sec
Stand-by current	Ist_V _{DD}		-	-	1	5	uA

6.2 Panel DC Characteristics

Notes: 1. The typical power is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern.



The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
 The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by WINSTAR Display.

4. Electrical measurement: Multimeter

6.3 AC Characteristics

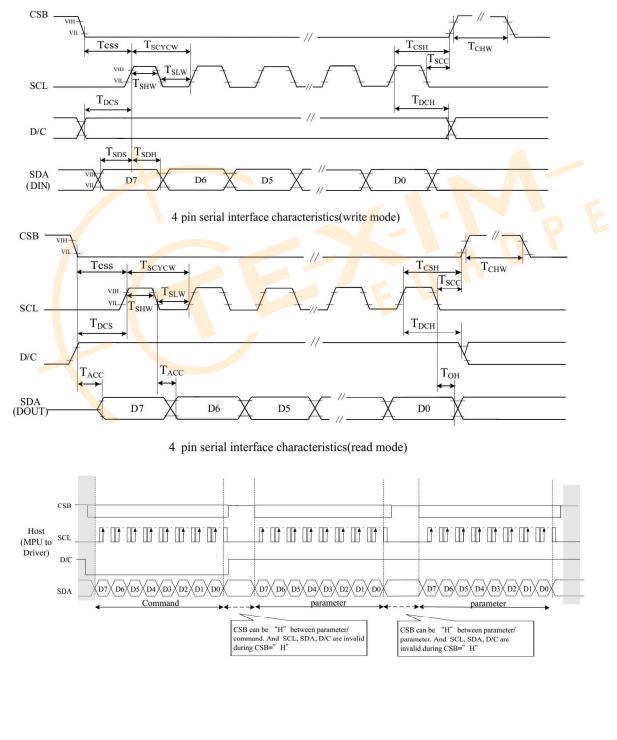
6.3.1 MCU Interface Selection

The 3-wire/4-wire serial port as communication interface for all the function and command setting.

3-wire/4-wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-wire/4-wire bus itself.

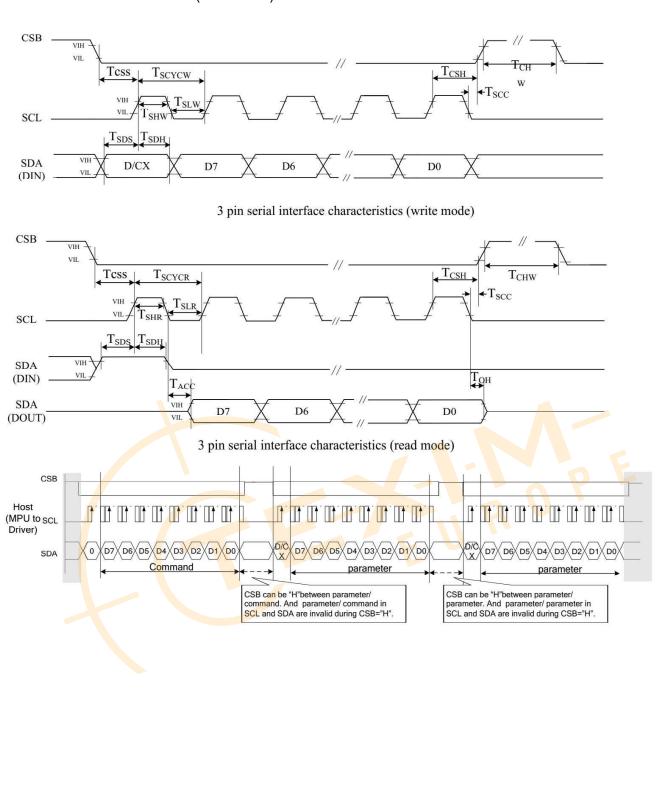
Under read mode, 3-wire/4-wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SCL by external controller. Data in the "Hi-Z phase" will be ignored by 3-wire/4-wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under "Hi-Z phase" and "Data phase".

6.3.2 MCU Serial Interface (4-wire SPI)



WINSTAR Display





7. Command Table

Addrose	command								E	Bit		
Address	command	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
		W	0	0	0	0	0	0	0	0	0	00H
R00H	Panel setting (PSR)	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
	C 63 (201)	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
		w	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-		-	-	VSC_EN	VDS_EN	VDG_EN	07h
		w	1	-		÷.	-	-	-	VGPN [1]	VGPN [0]	00h
R01H	Power setting (PWR)	w	1	-	VSPL_0[6]	VSPL_0[5]	VSPL_0[4]	VSPL_0[3]	VSPL_0[2]	VSPL_0[1]	VSPL_0[0]	00h
		W	1	-	VSP_1[6]	VSP_1 [5]	VSP_1 [4]	VSP_1 [3]	VSP_1 [2]	VSP_1 [1]	VSP_1 [0]	00h
		W	1	-	VSN_1[6]	VSN_1[5]	VSN_1[4]	VSN_1[3]	VSN_1[2]	VSN_1[1]	VSN_1[0]	00h
		w	1	-	VSPL_1[6]	VSPL_1[5]	VSPL_1[4]	VSPL_1[3]	VSPL_1[2]	VSPL_1[1]	VSPL_1[0]	00h
		w	0	0	0	0	0	0	0	1	0	02H
R02H	Power OFF(POF)	W	1	-	-	-	-	-	-	-	-	02h
D0411	D 01/0010											www.co.com
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
		W	0	0	0	0	0	0	1	1	0	06H
		W	1	-	-	-	-	PHB_S	SFT[1:0]	PHA_S	FT[1:0]	00h
		W	1	-	-			PHA_	ON[5:0]			02h
R06H	Booster Soft Start	w	1	17	1			PHA_0	OFF[5:0]			07h
Room	(BTST)	W	1	1	14			PHB_	ON[5:0]			02h
		W	1	-	-			PHB_0	OFF[5:0]			07h
		W	1	(-)		PHC_ON[5:0]						02h
		W	1	-	-			PHC_0	OFF[5:0]			07h
R07H	Deep Sleep(DSLP) Data Start	W	0	0	0	0	0	0	1	1	1	07H
RU/H		W	1	1	0	1	0	0	1	0	1	A5h
R10H		W	0	0	0	0	1	0	0	0	0	10H
RIUH	transmission (DTM)	W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	w	0	0	0	0	1	0	0	0	1	11H
KIIII		R	1	Data_flag		-		E I				-
R12H	Display Refresh	W	0	0	0	0	1	0	0	1	0	12H
111211	(DRF)	W	1			-		-		-		00H
R17H	Aut <mark>o</mark> sequence	W	0	0	0	0	1	0	1	1	1	17H
	(AUTO)	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
HOUT		W	1	14		2		Dyna		FR	[2:0]	02h
	Temperature Sensor	W	0	0	1	0	0	0	0	0	0	40H
R40H	Command (TSC)	R	1	D10/TS[7]	D9/TS[7]	D8/TS[6]	D7/TS[5]	D6/TS[4]	D5/TS[3]	D4/TS[2]	D3/TS[1]	
		R	1	D2/ TS[9]	D1/TS[8]	D0		-		ă.	171	
R41H	Temperature Sensor	W	0	0	1	0	0	0	0	0	1	41H
	Calibration (TSE)	W	1	TSE	-		TO[4]	TO[3]	TO[2]	TO[1]	TO0]	00h
		W	0	0	1	0	0	0	0	1	0	42H
R42H	Temperature Sensor	w	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
	Write (TSW)	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
	Temperature Sensor	w	0	0	1	0	0	0	0	1	1	43H
R43H	Read (TSR)	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	
R50H	VCOM and DATA	w	0	0	1	0	1	0	0	0	0	50H
10011	interval setting (CDI)	W	1	VBD[2]	VBD[1]	VBD[0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

R51H	Lower Power	W	0	0	1	0	1	0	0	0	1	51H
ROIN	Detection (LPD)	R	1	14	-	-		4	-	-	LPD	
		W	0	0	1	1	0	0	0	0	1	61H
		W	1	14	-	20	-	1	-	HRES(9)	HRES(8)	00h
R61H	Resolution	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
	setting(TRES)	w	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
		W	0	0	1	1	0	0	1	0	1	65H
		W	1	-	-	-		-	-	S_start(9)	S_start(8)	00h
R65H	Gate/Source Start	w	1	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00h
	Setting(GSST)	w	1	-			-	-	-	G_start(9)	G start(8)	00h
		w	1	G start(7)	G start(6)	G start(5)	G_start(4)	G start(3)	G start(2)	G_start(1)	G_start(0)	00h
		W	0	0	1	1	1	0	0	0	0	70H
		R	1	0	0	0	0	1	0	0	1	09h
R70H	REVISION (REV)	R	1	0	0	0	0	0	0	1	0	02h
		R	1	0	0	0	0	0	0	0	1	02h
				-								
R80H	Auto Measure Vcom	W	0	1	0	0	0	0	0	0	0	80 H
	(AMV)	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h
DOGU		w	0	1	0	0	0	0	0	0	1	81H
R81H	Vcom Value (VV)	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	
		w	0	1	0	0	0	0	0	1	0	82H
R82H	Vcom_DC Setting register(VDCS)	w	1	-						VDCS[1]		00h
		505	20		VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	1000000000000000	VDCS[0]	
		W	0	1	0	0	0	0	0	1	1	83H
	W	1	-	-	-	PTH_ENB	-	-	HRST(9)	HRST(8)	00h	
		W	1	HRST(7)	HRST(6)	HRST(5)	HRST(4)	HRST(3)	HRST(2)	0	0	00h
	-	W	1	-		-		-	-	HRED(9)	HRED(8)	00h
R83H	Partial Window (PTLW)	W	1	HRED(7)	HRED(6)	HRED(5)	HRED(4)	HRED(3)	HRED(2)	0 VR <mark>ST</mark> (9)	0	00h 00h
	(11200)	W	1	-	VRST(6)		- VRST(4)	VRST(3)	-		VRST(8) VRST(0)	00h
		w	1	VRST(7)	VKSI(0)	VRST(5)	VR31(4)	VR31(3)	VRST(2)	VRST(1) VRST(9)	VRST(0) VRST(8)	00h
		w	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(9)	VRST(0)	00h
		W	1	-	VK31(0)	VK31(3)	VK31(4)	-	VRST(2)	-	PMOD	00h
R90H	Program mode(PGM)	W	0	1	0	0	1	0	0	0	0	90H
	Active	and the second									25	100320120
R91H	Program(APG)	W	0	1	0	0	1	0	0	0	1	91H
R92H	R <mark>ea</mark> d MTP data	W	0	1	0	0	1	0	0	1	0	92H
13211	(RMTP)	R	1	#	#	#	#	#	#	#	#	
		W	0	1	0	1	0	0	0	1/	0	A2H
		W	1	-	-	-	VMTPSEL	-	= 1	M_dis	S_dis	00h
RA2H	MTP Program Config	W	1				PGM_SAD	DR[15:8]				00h
	Register(PGM_CFG)	W	1				PGM_SA					00h
		W	1				PGM_DS					0Fh
		W	1				PGM_DS		-	ř		00h
RE0H	CASCADE setting	W	0	1	1	1	0	0	0	0	0	E0H
and a state	(CCSET)	W	1	-	242	-	320	24	-	TSFIX	CCEIN	00h
RE3H	Power saving(PWS)	W	0		1 VCOM W	1		0	0	1	1	E3H
. LOIT	· owor ouving(i vvo)	W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h
DEAL	LVD voltage	W	0	1	1	1	0	0	1	0	0	E4H
RE4H	Select(LVSEL)	w	1	-	-	-			=	LVD_SEL [1]	LVD_SEL [0]	03h
RE5H	CASCADE setting select	W	0	1	1	1	0	0	1	0	1	E5H
	(CCS_SEL)					1	1	cascade_syn				

R00H		Bit									
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1 st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
2 nd Parameter	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

1 st paramet	Name	Description	
Bit	Indifie	Description RST_N function	
0	RST_N	1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and Source/Boder/Vcom: floating	
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and Source / Border / Vcom are kept 0V or floating. 1 : Booster on. (default)	
2	SHL	SHL function 0: Shift left; First data=Sn \rightarrow Sn-1 \rightarrow \rightarrow S2 \rightarrow Last data=S1. 1: Shift right: First data=S1 \rightarrow S2 \rightarrow \rightarrow Sn-1 \rightarrow Last data=Sn. (default)	
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →→G2→Last line=G1. 1:Scan up; First line=G1→G2 →→Gn-1→Last line=Gn. (default)	
5	PST_MODE	scanning.	
7-6	RES[1,0]	Resolution setting 00: Display resolution is 128x250(default) 01: Display resolution is 96x250 10: Display resolution is 64x250 11: Display resolution is 32x250	
 2 nd paramet	er		
Bit	Name	Description	
0	VC_LUTZ	VCOM status function 0 : No effect 1 : After refreshing display, the output of VCOM is set to floating automatically (default)	
1	NORG	VCOM status function 0 : No effect (default) 1 : After refreshing display, VCOM is tied to GND before power off	
2	TIEG	VGN power off status function 0 : No effect (default) 1 : Power off, VGN will be tied to GND	
3		Temperature sensing will be activated automatically one time 0 : Before enabling booster, Temperature Sensor will be activated automatically one time. 1 : When RST_N low to high, Temperature Sensor will be activated automatically one time. (default)	
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating	
5	FOPT	FOPT function 0: Scan 1 frame after waveform finished(default) 1: No scan after waveform finished and switch the source channel output to Hiz.	
7	LUT_EN	LUT selection setting 0 : Using LUT from MTP(default) 1 : Using LUT from register	
Priority of VC	COM setting: \	/CMZ > NORG > FOPT > VC_LUTZ	
FOPT setting		reshing display.	
 Dummy When SH VDD turn condition:(When RS² 	source line fol D_N become off.SD output a DV or floating. T_N become l	eep at VGN for DSP/DRF and AMV low LUTC for DSP/DRF ow, DCDC will turn off. Register and SRAM data will keep until and VCOM will base on previous condition. It may have two ow, driver will reset. All register will reset to default value. All of the able. Source/Gate/Border/VCOM will be released to floating	

las at /D						Bit					
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
st Parameter	W	1	-	-	-	1241	-	VSC_EN	VDS_EN	VDG_EN	07h
nd Parameter	W	1	-	2	-	-	-	-	VGPN [1]	VGPN [0]	00h
rd Parameter	w	1	-			V	SPL_0 [6	3:0]			00h
th Parameter	W	1	-			V	SP_1 [6	:0]			00h
th Parameter	W	1	3			V	'SN_1 [6	:0]			00h
6 th Parameter	W	1	-			V	SPL_1 [6	5:0]			00h
)TE: "-" Don't c	are ca	n be set	to VDD or	GND	evel						
escription			I defines a		0101						
escription	-116	Command	i dennes a	5.							
	1 st Pa	arameter									
		Bit	Nam	е			D	escription	า		
						r selection.					
		0	VDG_I	ΞN		al gate pow					
					1 : Interna	I DCDC fun	iction for	generate V	GP/VGN. (default)	
						wer selectio		VODA			
		1	VDS_I	ΞN		l source po				(default)	
								0.1.0.0.0		()	
		2	VSC_I	ΞN		power sele		VSPL nins			
		-				regulator fu				ault)	
	2nd F	Paramete	ALC: NO								
		Bit 💊	Nam	e			C	escriptio	n		
						tage Level. 20 v, VGN=-	20v (d	efault)			
	3	1-0	VGP	M	01: VGP=1			oldult)			
				N							
				•	10: VGP=1	5 v, VGN=-	15v				
					10: VGP=1 11: VGP=1	15 v, VGN=- 10 v, VGN=-	15v 10v				
	3rd &		n Parame		10: VGP=1 11: VGP=1	15 v, VGN=- 10 v, VGN=-	15v 10v	SPL_1 po	wer sele	ction	
		4th & 6t	n Parame		10: VGP=1 11: VGP=1	15 v, VGN=- 10 v, VGN=- P_1/VSPL	15v 10v 0/ VS		wer sele	ction	
	3rd & Bit		n Parame	ter: Inte	10: VGP=1 11: VGP=1 ernal VSF	15 v, VGN=- 10 v, VGN=- P_1/VSPL	-15v -10v 0/ VS		wer sele	ction	
		4th & 6t	n Parame	ter: Inte	10: VGP=1 11: VGP=1 ernal VSF	15 v, VGN=- 10 v, VGN=- P_1/VSPL	-15v -10v 0/ VS		wer seler	ction	
		4th & 6t	h Parame	ter: Inte VSP & V	10: VGP=1 11: VGP=1 ernal VSF /SPL powe	15 v, VGN=- 10 v, VGN=- P_1/VSPL De pr selection bit [6:	15v 10v 0/ VS escripti	on /oltage(V)	bit [6:0	Volta	
		4th & 6t	n Parame Internal	ter: Inte VSP & V 6:0]	10: VGP=1 11: VGP=1 vGP=1 /SPL power Voltage(V) 3	15 v, VGN=- 10 v, VGN=- 2_1/VSPL Depresent for selection bit [6: 0101001	15v 10v 0/ VS escripti	on /oltage(V) 7.1	bit [6:0]	Volta 52h 11	.2
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		4th & 6t	Internal	ter: Inter: Inter: Inter: Inter: 00 00h 00h 01 01h 01 01h 00h 11 03h 00 04h	10: VGP=1 11: VGP=1 ernal VSF /SPL powe Voltage(V 3 3.1 3.2	5 v, VGN=- 0 v, VGN=- P_1/VSPL Deer selection bit [6: 0101001 0101010	15v 10v 0/VS escripti 0] \ 29h 22h 2Bh	on /oltage(V) 7.1 7.2 7.3 7.4 7.5	bit [6:0] 1010010 1010011 1010011 1010100 1010101 1010110	Volta 52h 11 53h 11 54h 11	.2 .3 .4 .5 .6
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		4th & 6t	n Parame Internal bit 000000 000000 000000 000000 000000 0000	ter: Inter: Inter: Inter: Inter: 00 00h 00h 01 01h 01h 01h 01h 01h 01h 0	10: VGP=1 11: VGP=1 ernal VSF Voltage(V 3 3.1 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8	5 v, VGN=- 0 v, VGN=- 2 1/VSPL 0 to the selection 0 bit [6: 0101001 0101010 0101110 0101110 0101111 0101110 0101111 01011110 01011111 010111000 0110001	15v 10v 	on /oltage(V) 7.1 7.2 7.3 7.4 7.5 7.6 7.7 7.8 7.9	bit [6:0] 1010010 1010011 1010001 1010100 1010101 1010110 1011000 1011001 1011010	Volta 52h 11 53h 11 55h 11 55h 11 55h 11 56h 11 57h 11 58h 11 59h 11 5Ah 1	.2 .3 .4 .5 .6 .7 .8 .9 2
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	Bit	4th & 6t Nam	n Parame internal intern	VSP & 6:0] 00 01 01 01 01 01 01 01 01 02h 01 02h 03h 00 01 00 01 00 01 00 01 00 01 00 01 00 01 00 01 00 00 00 01 00 01 01 01 01 01 01 01 01 01 01 01 01 01	10: VGP=1 11: VGP=1 ernal VSF /SPL powe Voltage(V 3 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 3.6 3.7 3.8 3.9 4 4.1 4.2 4.3 4.4 4.5 4.6 4.7 4.8 4.9 5 5.1	5 v, VGN=- 0 v, VGN=- 0 v, VGN=- 2 1/VSPL 2 1/VSPL 2 1/VSPL 3 010101 0101001 0101010 0101011 0101010 0101111 010011 0110010 0110011 0110010 0110011 0110101 011011	15v 10v 20/ VS 29h 22h 22h 22h 22h 22h 22h 22h 30h 31h 32h 33h 33h 33h 33h 33h 33h 33h 33h 33	On 7.0ltage(V) 7.1 7.2 7.3 7.4 7.5 7.6 7.7 7.8 7.9 8 8.1 8.2 8.3 8.4 8.5 8.6 8.7 8.8 9 9.1 9.2	bit [6:0] 1010010 1010011 1010011 101000 1011011 1011001 1011001 1011001 1011011 101100 1011101 1011100 1011111 1100000 1100011 1100100 1100111 1100110 1100111	Volta 52h 11 53h 11 54h 11 55h 11 56h 11 57h 11 57h 11 58h 11 58h 12 57h 12 50h 12 55h 12 50h 12 50h 12 50h 12 50h 12 50h 12 60h 12 60h 12 60h 12 60h 13 66h 13 66h 13 67h 13	.2 .3 .4 .5 .6 .7 .8 .9 .2 2 .1 .1 .2 .3 .3 .4 .5 .6 .7 .8 .9 .2 .3 .3 .3 .4 .5 .5 .6 .3 .3 .3 .3 .3 .3 .3 .3 .3 .3 .3 .3 .3
	Bit	4th & 6t Nam	n Parame internal intern	VSP & 6:0] 00 01 01 01 01 01 01 01 01 01 01 01 02 03 04 05 06 01 02 03 04 05 06 07 08 01 02 03 04 05 06 07 08 01 02 03 04 05 06 07 07 08 09 01 01 02 03 04 05 04 <td>10: VGP=1 11: VGP=1 ernal VSF /SPL powe Voltage(V 3 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 3.9 4 4.1 4.2 4.3 4.4 4.5 4.6 4.7 4.8 4.9 5 5.1 5.2</td> <td>5 v, VGN=- 0 v, VGN=- 0 v, VGN=- 0 - 1/VSPL 0 - 1/VSPL</td> <td>15v 10v </td> <td>on 7.1 7.2 7.3 7.4 7.5 7.6 7.7 7.8 7.9 8 8.1 8.2 8.3 8.4 8.5 8.6 8.7 8.8 8.9 9 9.1 9.2 9.3</td> <td>bit [6:0] 1010010 1010010 1010010 1010100 1010101 1010100 1011011 1011000 1011011 1011001 1011101 1011100 1100001 1100100 1100101 1100100 1100111 1100100</td> <td>Volta 52h 11 53h 11 55h 11 55h 11 56h 11 57h 11 58h 11 58h 11 57h 11 58h 12 5Ch 12 5Ch 12 5Eh 12 60h 12 61h 12 63h 12 63h 12 64h 1 65h 12 66h 13 66h 13 66h 13 66h 13 67h 13 68h 13</td> <td>.2 .3 .4 .5 .6 .7 .8 .9 2 2 .1 .1 .2 .3 .3 .4 .5 .66 .7 .8 .9 2 .1 .1 .2 .3 .3 .4 .5 .5 .6 .6 .7 .7 .8 .9 .9 .2 .3 .3 .4 .5 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .8 .9 .2 .2 .5 .6 .6 .7 .7 .8 .8 .9 .2 .2 .5 .6 .6 .7 .7 .8 .8 .9 .2 .5 .6 .5 .6 .5 .7 .7 .8 .8 .9 .2 .5 .5 .6 .5 .7 .7 .8 .8 .9 .2 .4 .5 .5 .6 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5</td>	10: VGP=1 11: VGP=1 ernal VSF /SPL powe Voltage(V 3 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 3.9 4 4.1 4.2 4.3 4.4 4.5 4.6 4.7 4.8 4.9 5 5.1 5.2	5 v, VGN=- 0 v, VGN=- 0 v, VGN=- 0 - 1/VSPL 0 - 1/VSPL	15v 10v 	on 7.1 7.2 7.3 7.4 7.5 7.6 7.7 7.8 7.9 8 8.1 8.2 8.3 8.4 8.5 8.6 8.7 8.8 8.9 9 9.1 9.2 9.3	bit [6:0] 1010010 1010010 1010010 1010100 1010101 1010100 1011011 1011000 1011011 1011001 1011101 1011100 1100001 1100100 1100101 1100100 1100111 1100100	Volta 52h 11 53h 11 55h 11 55h 11 56h 11 57h 11 58h 11 58h 11 57h 11 58h 12 5Ch 12 5Ch 12 5Eh 12 60h 12 61h 12 63h 12 63h 12 64h 1 65h 12 66h 13 66h 13 66h 13 66h 13 67h 13 68h 13	.2 .3 .4 .5 .6 .7 .8 .9 2 2 .1 .1 .2 .3 .3 .4 .5 .66 .7 .8 .9 2 .1 .1 .2 .3 .3 .4 .5 .5 .6 .6 .7 .7 .8 .9 .9 .2 .3 .3 .4 .5 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .8 .9 .2 .2 .5 .6 .6 .7 .7 .8 .8 .9 .2 .2 .5 .6 .6 .7 .7 .8 .8 .9 .2 .5 .6 .5 .6 .5 .7 .7 .8 .8 .9 .2 .5 .5 .6 .5 .7 .7 .8 .8 .9 .2 .4 .5 .5 .6 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5
	Bit	4th & 6t Nam	n Parame internal intern	VSP & 6:0] 00 01 01 01 01 01 01 01 01 01 01 01 01 02 03 04 05 06 07 08 01 00 01 01 02 03 04 05 06 07 08 00 01 01 02 03 04 05 04 05 05 06 07 07 08 09 01 01 02 03	10: VGP=1 11: VGP=1 ernal VSF /SPL powe Voltage(V 3 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 3.9 4 4.1 4.2 4.3 4.4 4.5 4.6 4.7 4.8 4.9 5 5.1 5.2 5.3	5 v, VGN=- 0 v, VGN=- 0 v, VGN=- 0 - 1/VSPL 	15v 10v 	on 7.1 7.2 7.3 7.4 7.5 7.6 7.7 7.8 7.9 8 8.1 8.2 8.3 8.4 8.5 8.6 8.7 8.8 8.9 9 9.1 9.2 9.3 9.4	bit [6:0] 1010010 1010010 1010010 1010100 1010101 1010100 1011001 1011001 1011001 1011100 1011101 1001101 1100001 1100010 1100101 1100100 1100101 1100100 1100101	Volta 52h 11 53h 11 55h 11 55h 11 55h 11 57h 11 58h 11 57h 11 58h 11 58h 12 5Ch 12 5Ch 12 5Eh 12 5Fh 12 60h 12 61h 12 63h 13 66h 13 66h 13 67h 13 68h 13 69h 13	.2 .3 .4 .5 .6 .7 .8 .9 2 2 .1 .1 .2 .3 .3 .4 .5 .66 .7 .8 .9 .9 .3 .1 .5 .66 .7 .7 .8 .9 .9 .2 .3 .3 .4 .5 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .9 .2 .5 .6 .6 .7 .7 .8 .8 .9 .2 .5 .6 .6 .7 .7 .8 .8 .9 .2 .5 .6 .5 .6 .5 .6 .5 .6 .5 .6 .5 .6 .5 .7 .7 .8 .5 .5 .6 .5 .5 .5 .6 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5 .5
	Bit	4th & 6t Nam	n Parame internal bit 000000 000000 000000 000000 000000	VSP & 6:0] 00 01 01 01 01 01 01 01 01 01 01 01 02 03 04 05 06 01 02 03 04 05 06 07 08 01 02 03 04 05 06 07 08 01 02 03 04 05 06 07 07 08 09 01 01 02 03 04 05 04	10: VGP=1 11: VGP=1 ernal VSF /SPL powe Voltage(V 3 3.1 3.2 3.3 3.4 3.5 3.6 3.7 3.8 3.9 4 4.1 4.2 4.3 4.4 4.5 4.6 4.7 4.8 4.9 5 5.1 5.2	5 v, VGN=- 0 v, VGN=- 0 v, VGN=- 0 - 1/VSPL 0 - 1/VSPL	15v 10v 	on 7.0ltage(V) 7.1 7.2 7.3 7.4 7.5 7.6 7.7 7.8 7.9 8 8.1 8.2 8.3 8.4 8.5 8.6 8.7 8.8 8.9 9 9.1 9.2 9.3	bit [6:0] 1010010 1010010 1010010 1010100 1010101 1010100 1011011 1011000 1011011 1011001 1011101 1011100 100001 1100010 1100101 1100100 1100111 1100100 1100101	Volta 52h 11 53h 11 55h 11 55h 11 55h 11 57h 11 58h 11 57h 11 58h 11 58h 12 5Ch 12 5Ch 12 5Eh 12 5Fh 12 60h 12 61h 12 63h 13 66h 13 67h 13 66h 13 67h 13 68h 13 69h 13 69h 13 60h 13	.2 .3 .4 .5 .6 .7 .8 .9 2 .3 .4 .5 .6 .7 .8 .9 2 .3 .4 .5 .6 .7 .8 .9 3 .1 .2 .3 .4 .5 .6 .7 .8 .9 .3 .4 .5 .6 .7 .3 .4 .5 .6 .3 .4 .5 .6 .6 .6 .6 .6 .7 .6 .7 .7

11	I	0011010	1Ah	5.6	1000011	43h	9.7	1101100	6Ch	13.8	1 1
		0011011	1Bh	5.7	1000100	44h	9.8	101 V8-5251 V85 (*C. 1948) 84	6Dh	13.9	1
		0011100	1Ch	5.8	1000101	45h	9.9	1101110	6Eh	14	1
		0011101	1Dh	5.9	1000110	46h	10	1101111	6Fh	14.1	
		0011110	1Eh	6	1000111	47h	10.1	1110000	70h	14.2	1
		0011111	1Fh	6.1	1001000	48h	10.2	1110001	71h	14.3]
		0100000	20h	6.2	1001001	49h	10.3	1110010	72h	14.4	
		0100001	21h	6.3	1001010	4Ah	10.4		73h	14.5	
		0100010	22h	6.4	1001011	4Bh	10.5		74h	14.6	
		0100011	23h	6.5	1001100	4Ch	10.6		75h	14.7	4
		0100100	24h	6.6	1001101	4Dh	10.7		76h	14.8	
		0100101	25h	6.7	1001110	4Eh	10.8		77h	14.9	4
		0100110	26h	6.8	1001111	4Fh	10.9	1111000	78h	15	-
		0100111	27h	6.9	1010000	50h	11	other		15	
		0101000	28h	7	1010001	51h	11.1				
5th P	arameter:	Internal \	/SN_	1 power s	selection						
D''	New				5		tion				n
Bit	Name	Internal VS	N no	wer selectio		scrip	uon				4
		bit[6:0	-	Voltage(V)	bit [6:0	<u> </u>	Voltage(V)	bit [6:0]		Voltage(V)	
		0000000	00h	-3		29h	-7.1		52h	-11.2	
		0000001	01h	-3.1	0101010	2Ah	-7.2		53h	-11.3	
		0000010	02h	-3.2	0101011	2Bh	-7.3		54h	-11.4	
		0000011	03h	-3.3	0101100	2Ch	-7.4		55h	-11.5	
		0000100	04h	-3.4	0101101	2Dh	-7.5		56h	-11.6	
		0000101	05h	-3.5	0101110	2Eh	-7.6		57h	-11.7 -11.8	
		0000110	06h 07h	-3.6 -3.7	0101111 0110000	2Fh 30h	-7.7 -7.8	200 00 20 20 20 20	58h 59h	-11.8	
		0001000	08h	-3.8	0110000	31h	-7.9	1000 March 2000 March 2000	5Ah	-11.9	
		0001000	09h	-3.9	0110001	32h	-8		5Bh	-12.1	
		0001010	0Ah	-4	0110011	33h	-8.1		5Ch	-12.2	P
		0001011	0Bh	-4.1	0110100	34h	-8.2		5Dh	-12.3	
		0001100	0Ch	-4.2	0110101	35h	-8.3		5Eh	-12.4	
		0001101	0Dh	-4.3	0110110	36h	-8.4	1011111	5Fh	-12.5	
		0001110	0Eh	-4.4	0110111	37h	-8.5	1100000	60h	-12.6	
		0001111	0Fh	-4.5	0111000	38h	-8.6	1100001	<mark>6</mark> 1h	-12.7	
		0010000	10h	-4.6	0111001	39h	-8.7	1100010	62h	-12.8	
		0010001	11h	-4.7	0111010	3Ah	-8.8		63h	-12.9	
		0010010	12h	-4.8	0111011	3Bh	-8.9	Nach resolution of the second	64h	-13	
6-0	VSN_1	0010011	13h	-4.9	0111100	3Ch	-9		65h	-13.1	
		0010100	14h	-5	0111101	3Dh	-9.1		66h	-13.2	4
			15h	-5.1	0111110		-9.2		67h	-13.3	
		0010110	16h	-5.2	0111111	3Fh	-9.3	10 20 20200	68h	-13.4	4
		0010111	17h 18h	-5.3 -5.4	1000000	40h 41h	-9.4 -9.5		69h 6Ah	-13.5 -13.6	4
		0011000	18h	-5.4	1000001	41h 42h	-9.5		6An 6Bh	-13.6	1
		0011001	1Ah	-5.6	1000010	4211 43h	-9.0	1101011 6		-13.7	1
		0011010	1Bh	-5.7	1000100	44h	-9.8		6Dh	-13.9	1
		0011100	1Ch	-5.8	1000100	45h	-9.9		6Eh	-14	1
		0011101	1Dh	-5.9	1000110	46h	-10		6Fh	-14.1	1
		0011110	1Eh	-6	1000111	47h	-10.1		70h	-14.2	
		0011111	1Fh	-6.1	1001000	48h	-10.2	1110001	71h	-14.3	
		0100000	20h	-6.2	1001001	49h	-10.3	1110010	72h	-14.4	
		0100001	21h	-6.3	1001010	4Ah	-10.4	1110011	73h	-14.5	
		0400040	22h	-6.4	1001011	4Bh	-10.5	1110100	74h	-14.6	
		0100010			Succession and the	4Ch	-10.6	1110101	75h	-14.7	
		0100010	23h	-6.5	1001100	4011					
			23h 24h	-6.5 -6.6	1001100 1001101	4Dh	-10.7	1110110	76h	-14.8	
		0100011				2		1110111	77h	-14.8 -14.9	
		0100011 0100100 0100101 0100110	24h 25h 26h	-6.6 -6.7 -6.8	1001101 1001110 1001111	4Dh 4Eh 4Fh	-10.7 -10.8 -10.9	1110111			
		0100011 0100100 0100101	24h 25h	-6.6 -6.7	1001101 1001110	4Dh 4Eh 4Fh	-10.7 -10.8	1110111	77h	-14.9	- - - -

IOTTE: "-" Don't care, can be set to VDD or GND level -The command defines as : • After power off command, driver will power off base on power off sequence. • After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. • Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. • SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating. Restriction This command only active when BUSY_N = "1". R04H Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 Code		Notes:										
VSP VSP_0(+15) VSP_1(+3-+15) VSR_U(15) VSR_1(+3-+15) VSR_1(+3-+15) 3. If gate voltage is set to +1-15v, +1-10v, IC will auto correct source voltage as follows I. VGP- VSP_0/VSPL_0/VSP_1/VSPL_1>= 2v Image: Image		2. Wł Mo	nen swit de0: VS	ching Mod SP_0(+15	de0 or Mode) / VSN_0 (-	e1,the voltag 15) / VSPL_	e output 0 (+3~+1	15)	15)			
VSN VSN_0(16) VSN_1(3-16) VSPL_0(13) VSN_1(3-16) VSPL_1(-3-15) 3. If gate voltage is set to +1-15v, +1-10v, IC will auto correct source voltage as follows I, VGP-VSP_0 / VSPL_0 / VSPL_1 >= 2v II. VGN-VSN_0 / VSN_0 / VSPL_0 / VSPL_1 >= -2v For example: $ \frac{VSP_0}{VSP_0} + 15v + 15v + 16v + 16v $ Voltage $ \frac{VSP_0}{VSP_0} + 15v + 16v + 16v $ Voltage $ \frac{VSP_0}{VSP_0} + 15v + 16v + 16v $ Voltage $ \frac{VSP_0}{VSP_0} + 15v + 16v + 16v $ Voltage $ \frac{VSP_0}{VSP_0} + 15v + 16v + 16v $ Voltage $ \frac{VSP_0}{VSP_0} + 15v + 16v + 16v $ Voltage $ \frac{VSP_0}{VSP_0} + 15v + 16v + 16v $ Voltage $ \frac{VSP_0}{VSP_0} + 15v + 16v + 16v $ Voltage $ \frac{VSP_0}{VSP_0} + 15v + 16v + 16v $ Voltage $ \frac{VSP_0}{VSP_0} + 15v + 16v + 16v $ Voltage $ \frac{VSP_0}{VSP_0} + 15v $ Restriction $ \frac{NOCX}{O T O G O O O O O O O O O O O O O O O O $				N	1ode0	Mode1						
VSPL VSPL_0(+3-+15) VSPL_1(+3-+15) 3. If gate voltage is set to +/-15v, +/-10v, IC will auto correct source voltage as follows I. VGP- VSP_0 / VSP_0 / VSP_1 / VSPL_1 > = 2v II. VGN-VSN_0 / VSN_1 > = -2v For example: Image: transmission of the transmission of transmissi			VSP	VSF	P_0(+15)	VSP_1(+3~+15	5)					
3. If gate voltage is set to +/-15v, +/-10v, IC will auto correct source voltage as follows I. VGP- VSP_0 / VSP_0 / VSP_1 / VSPL_1 >= 2v II. VGN-VSN_0 / VSN_1 >= -2v For example: 												
Restriction Restriction Restriction		l	VSPL	VSPL_	0(+3~+15)	VSPL_1(+3~+1)	5)					
Note: Section: Color: Colo: Color: Color: Color: Colo: Color: Color: Co		I. VG II. VG	BP- VSP GN- VSI	_0 / VSPI N_0 / VSN	L_0/VSP_*			rrect soui	ce volta	ge as foll	ows	
Restriction Restriction -The command defines as :				symbol	Voltage setting	Real Voltage	1					
Rock R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 Code astriction				10.0000000	7900							
Voltage VSN_0 -15v -4v Voltage VSN_1 -5v -5v VCOMH +15v+(-2v) +8v+(-2v) VCOML -15v+(-2v) -2v vcomb -2v -2v Rozet Marcet 0							-					
Restriction Vision of the power off command, driver will power off base on power off sequence. After power off command, driver will power off base on power off sequence. After power off command, driver will power off base on power off sequence. After power off command, driver will power off base on power off sequence. After power off command, driver will power off base on power off sequence. After power off command, driver will power off base on power off sequence. After power off command, driver will power off base on power off sequence. After power off command, driver will power off base on power off sequence. After power off command, BUSY_N signal will rise from low to high. Power off command, BUSY_N signal will keep until VDD off. So utput and VCOM will base on previous condition. It may have two conditions: 0v or floating. Restriction This command only active when BUSY_N = "1". Roth Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D5 D4 D6 D5 D7 D6 D6 D5 D4 D3 D5 D4 D3 D6							-					
Voltage VSN_1 -5v -5v VSPL +15v +8v +8v VCOMH +15v+(-2v) +8v+(-2v) +8v VCOMDC -2v -2v -2v Restriction Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 Code POF W 0 0 0 0 0 1 0 02H ** Parameter W 0 - - - - 00<				VSP 1			1					
Image: Non-structure VCOMH +15v+(-2v) +8v +(-2v) VCOML -15v+(-2v) -2v -2v Restriction Bit Image: Non-structure Difference Inst/Para RW D/CX D7 D6 D5 D4 D3 D2 D1 D0 Code POF W 0 0 0 0 0 1 0 02H at parameter W 0 - - - - - 00 OTE: "-" Don' care, can be set to VDD or GND level D - - - - 00 Description -The command defines as : - - - - - 00 Poer off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N signal will drop from high to low. When finish the power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating. Restriction This command only active when BUSY_N = "1". - - - - - - -			Voltage				1					
VCOML -15vr(-2v) -8v + (-2v) Restriction -2v -2v Restriction Bit Discrete Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 Code POF W 0 0 0 0 0 1 0 02H ** Parameter W 0 - - - - - 00 DTE: ** Don't care, can be set to VDD or GND level - - - - 00 Description -The command defines as : - - - - 00 Power off command, driver will power off base on power off sequence. - After power off command, BUSY_N signal will rise from low to high. - Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. - SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating. Restriction This command only active when BUSY_N = "1". - - - - - - - - - - - <td></td> <td></td> <td></td> <td>10 10 10</td> <td>Metropolo</td> <td></td> <td>-</td> <td></td> <td></td> <td></td> <td></td> <td></td>				10 10 10	Metropolo		-					
VCOMDC2v Restriction Restriction Restriction Restriction NOT care, can be set to VDD or GND level OPE: *-" Don't care, can be set to VDD or GND level Description - The command defines as : • After power off command, driver will power off base on power off sequence. • After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N signal will rise from low to high. • Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. • SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating. Restriction This command only active when BUSY_N = "1". Restriction This command only active when BUSY_N = "1".				The residue of the second second		. 07 (176) 	4					
Restriction Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 Code POF W 0 0 0 0 0 0 1 0 02H at Por W 0 - - - - - 00 at Por W 0 - - - - - 00 at port care, can be set to VDD or GND level - - - - - 00 Description -The command defines as : - - - - - 00 After power off command, driver will power off base on power off sequence. After power off command, BUSY_N signal will drop from high to low. When finish the power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating. Restriction This command only active when BUSY_N = "1". Ether the sethetter the sethetter the sethetter the sethetter the sethetter term of term of t							1					
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DTE: "-" Don't care, can be set to VDD or GND level Description -The command defines as : • After power off command, driver will power off base on power off sequence. • After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. • Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. • SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating. Restriction This command only active when BUSY_N = "1". R04H Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 Code		R/W	D/CX	D7	D6 D		D3	D2	D1	D0	Code	
Description -The command defines as : • After power off command, driver will power off base on power off sequence. • After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. • Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. • SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating. Restriction This command only active when BUSY_N = "1". R04H Bit Inst/Para R/W R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 Code	Inst/Para POF	W	0			5 D4					02H	
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R04H Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 Code	Inst/Para POF st Parameter OTE: "-" Don't c	W W are, can be	0 0 set to V	0 - DD or GND	0 0	5 D4					02H	
Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 Code	Inst/Para POF I st Parameter OTE: "-" Don't co Description	W W are, can be -The comn After After powe Powe temp SD c floati	0 set to Vinand def	0 - DD or GNL fines as : off comma off comma quence, E mmand v sensor, b nd VCOM	0 0 D level and, driver v and, BUSY_N and, BUSY_N sin vill turn off c but register a will base of	5 D4 0 - N signal will gal will rise f harge pump, and SRAM d n previous co	0 - drop fro from low , T-con, s ata will k	0 - om high to to high. source dr ceep until	1 - off seque o low. W iver, gat VDD off	nce. hen finisl e driver,	02H 00 h the VCOM,	
	Inst/Para POF I st Parameter OTE: "-" Don't co Description	W W are, can be -The comn After After powe Powe temp SD c floati	0 set to Vinand def	0 - DD or GNL fines as : off comma off comma quence, E mmand v sensor, b nd VCOM	0 0 D level and, driver v and, BUSY_N and, BUSY_N sin vill turn off c but register a will base of	5 D4 0 - N signal will gal will rise f harge pump, and SRAM d n previous co	0 - drop fro from low , T-con, s ata will k	0 - om high to to high. source dr ceep until	1 - off seque o low. W iver, gat VDD off	nce. hen finisl e driver,	02H 00 h the VCOM,	
	Inst/Para POF I st Parameter OTE: "-" Don't co Description Restriction	W W are, can be -The comn After Powe Powe temp SD c floati	0 set to Vinand def power power proff se er off se er off se porture poutput an ng.	0 - DD or GNL ines as : off comma off comma quence, E ymmand w sensor, b ad VCOM	o o o level and, driver v and, BUSY_N and, BUSY_N sin vill turn off c but register a will base of will base of	5 D4 0 - will power off N signal will gal will rise f harge pump and SRAM d n previous co	0 - f base or l drop fro from low , T-con, ş ata will k ondition.	0 - om high to to high. source dr teep until It may ha	1 	0 hen finisl e driver, f. condition	02H 00 h the VCOM, s: 0v or	
NOTE: "-" Don't care, can be set to VDD or GND level	Inst/Para POF I st Parameter OTE: "-" Don't co Description Restriction Restriction	W W are, can be -The comn After Powe Powe temp SD c floati	0 set to Vinand def power power power power off co perature putput an ng.	0 - DD or GNL ines as : off comma off comma off comma off comma wmmand w sensor, b ad VCOM Ily active w	0 0 - - 0 level and, driver values of and, BUSY_N single for a single state of a single s	5 D4 0 - will power off N signal will gal will rise f harge pump, and SRAM d n n previous co f	0 - f base or l drop fro from low , T-con, ; ata will k ondition.	0 - om high to to high. source dr teep until It may ha	1 	0 - nce. hen finisl e driver, f. condition	02H 00 h the VCOM, s: 0v or	
 -The command defines as : After power on command, driver will power on base on power on sequence. After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence (base on PWR command), BUSY_N signal will rise from low to 	Inst/Para POF st Parameter DTE: "-" Don't c. Description Restriction Restriction Restriction Inst/Para PON	W W are, can be -The comn After After Powe temp SD c floati	0 0 set to V nand def power power power off se er off se er off se er off se ner off se ner off se ner off se power power ner off se ner off se ner off se power Dutput an ng. D/CX 0	0 - DD or GNL ines as : off comma off comma off comma yensor, b and VCOM ly active yent D7 0	0 0 - - D level and, driver values of and, BUSY_N sime	5 D4 0 - will power off N signal will gal will rise f harge pump and SRAM d n previous co	0 - f base or l drop fro from low , T-con, ş ata will k ondition.	0 - om high to to high. source dr teep until It may ha	1 	0 hen finisl e driver, f. condition	02H 00 h the VCOM, s: 0v or	
high.	Inst/Para POF I st Parameter OTE: "-" Don't co Description Restriction Restriction	W W are, can be -The comn • After powe Powe • Powe temp • SD c floati	0 0 set to V nand def power power power output a ng. D/CX 0 e set to V nmand def power	0 - DD or GNL ines as : off comma off comma off comma off comma yearsor, b mmand w sensor, b nd VCOM Iy active w D7 0 //D or GNL efines as r on comma r on comma	0 0 - - D level - and, driver vand, BUSY_Asing - 3USY_N sing - vill turn off court register asing - will base of - when BUSY - D6 0 D level - : - mand, driver vand, BUSY	5 D4 0 - will power off - N signal will gal will rise f harge pump - and SRAM d - n previous co - <u>CN = "1".</u> - Bit - D5 D4 0 0	0 - f base or drop fro from low , T-con, s ata will k ondition.	0 	1 off seque b low. W iver, gat VDD off ave two D1 0 sequen to low. V	0 	02H 00 VCOM, s: 0v or Code 04H	

R06H						Bit					
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1 st Parameter	W	1	-	-	-	-	PHB_SFT [PHA_	SFT [1:0]	00h
2 nd Parameter	W	1	-	-	-		PHA_ON [5:	1750) C. 1940			02h
3 rd Parameter	W	1	-	-			PHA_OFF [5				07h
4 th Parameter	W	1	-	-			PHB_ON [5:	0]			02h
5 th Parameter	W	1	-	-			PHB_OFF [5	:0]			07h
6 th Parameter	W	1	-	-			PHC_ON [5	0]			02h
7 th Parameter	W	1		-			PHC_OFF [5	:0]			07h
		urrent	nd define mode and Name	d Cons	stant On Ti	Des period of ph	etting by JD cription nase A:	CMD			
	1-0		PHA_SF	T (, ,	00: 10mS 01: 20mS 10: 30mS 11: 40mS Soft start ((default)	ase B.				
	3-2		PHB_SF	-т <mark>(</mark>	00: 10mS 01: 20mS 10: 30mS 11: 40mS						
			Bit[5:0]	De	escription	Bit[5:0]	Descriptio	n Bit	t[5:0]	Descriptio	n
			000000	s	strength1	010110	strength23	10	01100	strength45	5
			000001	s	strength2	010111	strength24	10)1101	strength46	5
			000010	S	strength3	011000	strength25	10	01110	strength47	
			000011	s	strength4	011001	strength26	10	01111	strength48	3
Description			000100	s	strength5	011010	strength27	11	0000	strength49)
			000101	s	strength6	011011	strength28	11	0001	strength50)
	×		000110	s	strength7	011100	strength29	11	0010	strength51	
			000111	S	strength8	011101	strength30	11	0011	strength52	2
			001000	s	strength9	011110	strength31	11	0100	strength53	3
	Drivir		001001	st	trength10	011111	strength32	11	0101	strength54	
	strengt PHA O		001010	st	trength11	100000	strength33	11	0110	strength55	5
			001011	st	trength12	100001	strength34	11	0111	strength56	5
	PHB O	N & L			acinguniz		Suenguio4				1
			001100		trength13	100010	strength35	11	1000	strength57	·
	PHB O			s			-		1000 1001	strength57 strength58	
	PHB O		001100	st	trength13	100010	strength35	11	NO. 14 . N		3
	PHB O		001100 001101	si si	trength13 trength14	100010 100011	strength35 strength36	11	1001	strength58	3
	PHB O		001100 001101 001110	si si si	trength13 trength14 trength15	100010 100011 100100	strength35 strength36 strength37	11 11 11	1001 1010	strength58 strength59	})
	PHB O		001100 001101 001110 001111	si si si si	trength13 trength14 trength15 trength16	100010 100011 100100 100101	strength35 strength36 strength37 strength38	11 11 11 11	1001 1010 1011	strength58 strength59 strength60	3))
	PHB O		001100 001101 001110 001111 010000	st st st st st	trength13 trength14 trength15 trength16 trength17	100010 100011 100100 100101 100110	strength35 strength36 strength37 strength38 strength39	11 11 11 11 11 11	1001 1010 1011 1100	strength58 strength59 strength60 strength61	3)) 2
	PHB O		001100 001101 001110 001111 010000 010001		trength13 trength14 trength15 trength16 trength17 trength18	100010 100011 100100 100101 100110 100111	strength35 strength36 strength37 strength38 strength39 strength40	11 11 11 11 11 11 11	1001 1010 1011 1100 1101	strength58 strength59 strength60 strength61 strength62	3)) 2 3
	PHB O		001100 001101 001110 001111 010000 010001 010001	si si si si si si si si si	trength13 trength14 trength15 trength16 trength17 trength18 trength19	100010 100011 100100 100101 100110 100111 101000	strength35 strength36 strength37 strength38 strength39 strength40 strength41	11 11 11 11 11 11 11 11	1001 1010 1011 1100 1101 1101	strength58 strength60 strength60 strength62 strength63	3)) 2 3

Description			Bit[5:0)] Des	cription	Bit[5:0]	Des	cription	Bit[5:0]	Descript	ion
			00000) Pe	eriod1	010110	Pe	eriod23	101100	Period4	5
			00000	1 Po	eriod2	010111	Po	eriod24	101101	Period4	6
			00001) Pe	eriod3	011000	Pe	eriod25	101110	Period4	7
			00001	I Pe	eriod4	011001	Pe	eriod26	101111	Period4	8
			00010) Pe	eriod5	011010	Pe	eriod27	110000	Period4	9
			00010	1 Pe	eriod6	011011	Pe	eriod28	110001	Period5	0
			000110) Pe	eriod7	011100	Pe	eriod29	110010	Period5	1
			00011	l Pe	eriod8	011101	Pe	eriod30	110011	Period5	2
		linimum FF time	00100) Pe	eriod9	011110	Pe	eriod31	110100	Period5	3
		etting of	00100	1 Pe	riod10	011111	Pe	eriod32	110101	Period5	4
		HA_OFF	001010) Pe	riod11	100000	Pe	eriod33	110110	Period5	5
		&	00101	l Pe	riod12	100001	Pe	eriod34	110111	Period5	6
		HB_OFF	001100) Pe	riod13	100010	Pe	eriod35	111000	Period5	7
	PH	& IC OFF	00110	l Pe	riod14	100011	Pe	eriod36	111001	Period5	8
			001110) Pe	riod15	100100	Pe	eriod37	111010	Period5	9
			001111	Pe	riod16	100101	Pe	eriod38	111011	Period6	0
			01000) Pe	riod17	100110	Pe	eriod39	111100	Period6	1
			01000	1 Pe	riod18	100111	Pe	eriod40	111101	Period6	2
			01001) Pe	riod19	101000	Pe	priod41	111110	Period6	3
			01001	l Pe	riod20	101001	Pe	eriod42	111111	Period6	4
			01010) Pe	riod21	101010	Pe	eriod43			
			01010	1 Pe	riod22	101011	Pe	eriod44			
Restriction											A
R07H	R/W	D/CX	D7	D6	D5	Bit D4	D3	D2	D1	D0	Code
R07H	R/W W	D/CX 0	D7 0	D6 0	D5 0	Bit D4 0	D3 0	D2	D1 1	D0 1	Code 07H
R07H Inst/Para DSLP						D4			1		the second se
R07H Inst/Para DSLP ^t Parameter	W W	0	0	0	0	D4 0	0	1	1	1	07H
R07H Inst/Para DSLP ^t Parameter DTE: "-" Don't	W W care, car	0 1 n be set t	0	0 0 GND level	0	D4 0	0	1	1	1	07H
R07H Inst/Para DSLP ^t Parameter DTE: "-" Don't	W W care, car The co	0 1 <i>be set t</i> omma <mark>n</mark> d	0 1 0 VDD or 0 define as	0 0 GND level follows:	0	D4 0 0	0	1	1		07H A5h
R07H Inst/Para DSLP ^t Parameter DTE: "-" Don't	W W care, car The co After th	0 1 be set t pmmand	0 1 VDD or 0 define as	0 0 GND level follows:	0 1 d, the chi	D4 0 0	0 0 enter th	1 1 e deep-	1		07H A5h
R07H Inst/Para DSLP ^t Parameter DTE: "-" Don't	W W care, car The co After th The de	0 1 ommand nis comr	0 1 0 VDD or 0 define as nand is tra 0 mode w	0 0 GND level follows: ansmitted ould retu	0 1 d, the chi rn to sta	D4 0 0	0 0 enter th nardwa	1 1 e deep- re reset.	1	to save p	07H A5h bower.
R07H Inst/Para DSLP Parameter DTE: "-" Don't	W W care, car The co After th The de	0 1 ommand his comr eep sleep	0 1 0 VDD or 0 define as nand is tra 0 mode w	0 0 GND level follows: ansmitted ould retu	0 1 d, the chi rn to sta	D4 0 0	0 0 enter th nardwa	1 1 e deep- re reset.	1 0 sleep mode	to save p	07H A5h bower.
R07H Inst/Para DSLP ^t Parameter DTE: "-" Don't	W Care, car The co After th The de The or	0 1 ommand his comr eep sleep	0 1 0 VDD or 0 define as nand is tra 0 mode w	0 0 GND level follows: ansmitted ould retu	0 1 d, the chi rn to sta	D4 0 0	0 0 enter th nardwa	1 1 e deep- re reset.	1 0 sleep mode	to save p	07H A5h bower.
R07H Inst/Para DSLP st Parameter DTE: "-" Don't Description	W W care, car The cc After th The de The or 0xA5.	0 1 ommand his comm eep slee hly one p	0 1 0 VDD or 0 define as nand is tra 0 mode w	0 0 GND level follows: ansmitted ould retu is a chec	0 1 d, the chi rn to sta ck code,	D4 0 0	0 0 enter th nardwa	1 1 e deep- re reset.	1 0 sleep mode	to save p	07H A5h bower.
R07H Inst/Para DSLP at Parameter DTE: "-" Don't Description	W W care, car The cc After th The de The or 0xA5.	0 1 ommand his comm eep slee hly one p	0 1 o VDD or 0 define as nand is tra o mode w arameter	0 0 GND level follows: ansmitted ould retu is a chec	0 1 d, the chi rn to sta ck code,	D4 0 0	0 0 enter th nardwa	1 1 e deep- re reset.	1 0 sleep mode	to save p	07H A5h bower.
R07H Inst/Para DSLP ** Parameter DTE: *-" Don't Description Restriction	W W care, car The cc After th The de The or 0xA5.	0 1 n be set t pommand his comr pep sleep sleep sleep sleep sleep sleep sleep sleep	0 1 define as nand is tra o mode w arameter	0 0 GND level follows: ansmitted ould retu is a chec	0 1 d, the chi rn to sta ck code,	D4 0 0 ip would e ndby by h the comm	0 0 enter th nardwa	1 1 e deep- re reset.	1 0 sleep mode	to save p	07H A5h bower.
R07H Inst/Para DSLP t Parameter DTE: "-" Don't Description Restriction Restriction R10H Inst/Para TM_master	W W care, car The cc After th The de The or 0xA5. This cc R/W D W	0 1 n be set t pommand his comr pep sleep sleep sleep sleep sleep sleep sleep sleep	0 1 define as nand is tra o mode w arameter only activ	0 0 6ND level follows: ansmitted ould retu is a cheo re when	0 1 d, the chi rn to sta ck code, BUSY_N D5 0	D4 0 0 ip would e ndby by h the comr N = "1". Bit D4 1	0 0 enter th nardwa mand w	e deep- re reset. ould be	1 0 sleep mode excited if c D1 0	to save p heck code	07H A5h power. = Code 10H
R07H Inst/Para DSLP t Parameter DTE: "-" Don't Description Restriction Restriction R10H Inst/Para TM_master	W W care, car The cc After th The de The or 0xA5. This cc R/W D	0 1 n be set t pommand nis comr eep sleep sleep sleep sleep sleep sleep	0 1 define as nand is tra o mode w arameter only activ	0 0 6ND level follows: ansmitted ould retu is a cheo re when	0 1 d, the chi rn to sta ck code, BUSY_N	D4 0 0 ip would e ndby by h the comr N = "1". Bit D4 1	0 0 enter th nardwa mand w	e deep- re reset. ould be	1 0 sleep mode excited if c D1 0	e to save p heck code	07H A5h power. =
R07H Inst/Para DSLP ** Parameter DTE: "-" Don't Description Restriction Restriction Restriction R10H Inst/Para TM_master	W W care, car The cc After th The de The or 0xA5. This cc R/W D W	0 1 n be set t pommand nis comr eep sleep ply one p pommand //CX 0	0 1 define as nand is tra o mode w arameter only activ	0 0 6ND level follows: ansmitted ould retu is a cheo re when	0 1 d, the chi rn to sta ck code, BUSY_N D5 0	D4 0 0 ip would e ndby by h the comr N = "1". Bit D4 1	0 0 enter th nardwa mand w	e deep- re reset. ould be	1 0 sleep mode excited if c D1 0	to save p heck code	07H A5h power. = Code 10H
R07H Inst/Para DSLP ^t Parameter DTE: "-" Don't Description Description Restriction R10H Inst/Para TM_master st Parameter 	W W care, car The cc After th The de The or 0xA5. This cc R/W D W W W	0 1 n be set t pmmand nis comr pep sleep ply one p pmmand //CX 0 1 1 1	0 1 define as nand is tra o mode w arameter only activ 0 <u>Pixel1</u> : Pixel(n-3)	0 0 6ND level follows: ansmitted ould retu is a cheo //e when	0 1 1 d, the chi rn to sta ck code, BUSY_N <u>D5</u> 0 Pixel : : Pixel(n	D4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 enter th hardwa mand w D3 0 F	e deep- re reset. ould be	1 0 sleep mode excited if c	to save p heck code	07H A5h power. = Code 10H 00h
R07H Inst/Para DSLP ^{at} Parameter DTE: "-" Don't Description Restriction Restriction Restriction Restriction Inst/Para TM_master ^{at} Parameter	W W care, car The cc After th The de The or 0xA5. This cc R/W D W W W	0 1 n be set t pmmand nis comr pep sleep ply one p pmmand //CX 0 1 1 1	0 1 define as nand is tra o mode w arameter only activ 0 <u>Pixel1</u> : Pixel(n-3)	0 0 6ND level follows: ansmitted ould retu is a cheo //e when	0 1 1 d, the chi rn to sta ck code, BUSY_N <u>D5</u> 0 Pixel : : Pixel(n	D4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 enter th hardwa mand w D3 0 F	1 1 1 e deep- re reset. ould be D2 0 ixel3 :	1 0 sleep mode excited if c	to save p heck code	07H A5h oower. = <u>Code</u> 10H 00h 00h
R07H Inst/Para DSLP at Parameter DTE: "-" Don't Description Restriction Restriction Restriction Restriction Inst/Para TM_master 1st Parameter : : : :	W W care, cal The cc After th The de The or 0xA5. This cc R/W D W W W W W W W	0 1 n be set t pmmand nis command pep sleep poly one p pmmand //CX 0 1 1 1 1 1 1 1	0 1 define as nand is tra o mode w arameter only activ 0 <u>Pixel1</u> : Pixel(n-3)	0 0 6ND level follows: ansmitted ould retu is a cheo ve when 0 0 0	0 1 1 d, the chi rn to sta ck code, BUSY_N <u>D5</u> 0 Pixel : : Pixel(n	D4 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 enter th hardwa mand w D3 0 F	1 1 1 e deep- re reset. ould be D2 0 ixel3 :	1 0 sleep mode excited if c	to save p heck code	07H A5h oower. = <u>Code</u> 10H 00h 00h
R07H Inst/Para DSLP ** Parameter DTE: "-" Don't Description Restriction	W W care, cal The cc After th The de The or 0xA5. This cc R/W D W W W W W W Care, cal The co The co	0 1 n be set t pmmand nis comr pep sleep ply one p pmmand VCX 1	0 1 define as nand is tra o mode w arameter only activ 0 Pixel1 : : Pixel(n-3) o VDD or C define as indicates	0 0 6ND level follows: ansmitted ould retu is a cheo ve when 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 1 1 1	D4 0 0 ip would endby by here ndby by here the common set of	0 0 enter th nardwa mand w D3 0 F	e deep- re reset. ould be <u>D2</u> 0 ixel3 : : el(n-1)	1 0 sleep mode excited if c	to save p heck code	07H A5h power. = Code 10H 00h 00h

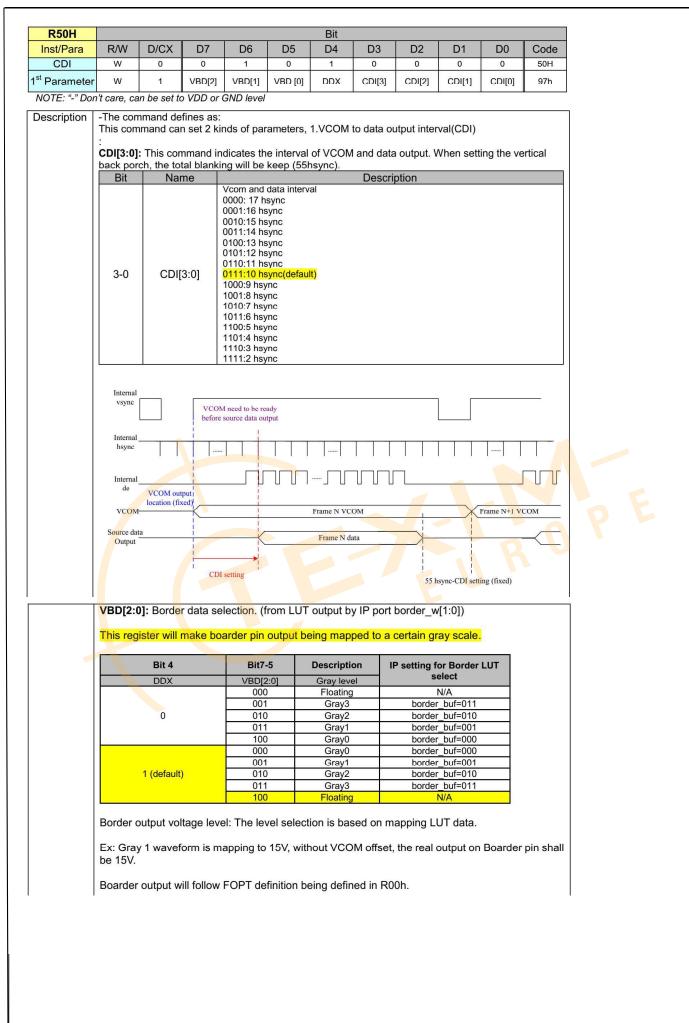
R17H Inst/Para to Sequence Parameter	succes reduce includi	the com ng PON,	cution ca plexity of DRF, PC	n minimi: host's co F, DSLF	D5 0 Code[5] I sequenc ze idle tir ontrol pro 2. DN→DRF	ne to avo ocedure.	id unnec	essary p	ower cor	nsumption	n and
R17H Inst/Para uto Sequence Parameter	W W The com succes reduce	0 1 mand car sive exec the com	0 Code[7] enable th cution ca plexity of	0 Code[6] ne internal n minimi: host's co	0 Code[5] I sequenc ze idle tir ontrol pro	1 Code[4] ce to exec ne to avo	0 Code[3] cute seve	1 Code[2] eral comr essary p	1 Code[1] mands co ower cor	1 Code[0] ontinuous	17H A5h sly. The n and
R17H Inst/Para uto Sequence Parameter	W W The com	0 1 mand car	0 Code[7] enable th	0 Code[6] ie internal	0 Code[5] sequenc	1 Code[4] ce to exec	0 Code[3] cute seve	1 Code[2] eral comr	1 Code[1] mands co	1 Code[0]	17H A5h sly. The
R17H Inst/Para Ito Sequence	W	0	0	0	0	1	0	1	1	1	17H
R17H Inst/Para			2.5 State 10 State 2.5 Sta							the stream of the	
					DE		D2	Da	D1	D 0	
estriction					-	Bit					
	This co	mmand or	nly active	s when B	USY_N =	: "1"					
		splay refre	esh comm	and, BU	SY_N sig	nal will be	ecome "0'	**			
	While u LUT.	sers send	I this com	mand, dr	iver will re	efresh dis	play (dat	a/VCOM)	base on	SRAM da	ata and
	R12h=0										
escription	-The co	mmand d	efines as	:							
^{it} Parameter DTE: "-" Don'i		1 1 be se <mark>t t</mark> o	- VDD or G	- ND level	-	-	-	-	-	-	00h
DRF	W	0	0	0	0	1	0	0	1	0	12H
R12H Inst/Para	R/W	D/CX	D7	D6	D5	Bit D4	D3	D2	D1	D0	Code
striction	THIS COL	ninano or	ny actives	when B	USY_N =						
					reshing o		tarts.				
	After "D	ata Start	" (10h) oi	"Data S	top" (11h) comma	inds and	when da	ta_flag=	1, <mark>BUSY</mark>	N
				1: Drive	er has alr	eady rec	eived all	or the on	e trame	uata.	
	7	Dat	ta_flag		er didn't r				- fr	dat-	
	Bit		lame			C	escriptio	n			
	Da 1ª Parar		normation								
Joonpuon	• W	hile finish		ta transn	nitting, us	er must s	end this c	command	to driver	and read	ł
TE: "-" Don't			VDD or G efines as								
Parameter	R		Data_flag	-	-	-	-	-	-	-	-
DSP	W	0	0	0	0	1	0	0	0	1	11H
R11H nst/Para	R/W	D/CX	D7	D6	D5	Bit D4	D3	D2	D1	D0	Code
estriction				_		D ¹¹					
	port"og										
	When [DX=0,P	ixel[1:0]=	11 ->Gra	y level s	elect=Gra	ay0,follov	v LUT da	ita output	t from IP	output
	port"og	ray01".									
	When [DDX=1,P		01 ->Gra	ay level s	elect=Gra	ay1,follov	w LUT da	ata outpu	t from IP	output
	Data m	apping e	xample:								
	11	b	Gray	3	ogra	ay03		Gray0		ogray00	D
	10)b	Gray	2	ogra	ay02		Gray1		ogray01	1
	01	lb	Gray			ay01		Gray2		ogray02	
	00		Gray		73	ay00	Giay	Gray3		ogray03	
	Pixel	Data	Gray level		(default)	LUT select	Cro	y level sele	DDX=0	output LUT	- coloct

Inst/Para PLL ^t Paramete					-		Bit					
Paramete		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
aramete		W W	0	0	0	1	1	0 Dyna	0 FR[2]	0 FR[1]	0 FR[0]	30H 02h
'E: "-" Dor	n't care	e, can t		VDD or G	ND level	-		Dyna	T N[2]	T N[1]	r R[0]	0211
cription	-The	comm	nand def	ines as:								
	12 (180)/20											
		comm le rate		ntrols the	PLL cloc	k freque	ncy. The	PLL strue	cture mus	st suppor	t the follo	wing
		e fate	0.									
					b	it3 Dy	/namic frar	ne rate				
						0 Di	sable(defa	ult)				
	1000					1 Er	nable					
	Note		rame ra	to								
	0: Fr	rame r	ate will	being de	fined in F							
	1: Fr	ame r	ate will	being de	fined by I	R20h(LU	T).					
					FR	[2:0] F	rame rate					
					-		2.5 Hz					
					-		i Hz		_			
							Hz(defaul	t)				
							i Hz					
							i Hz					
					1	01 85	i Hz					
					1		00 Hz					
					1	11 12	20 Hz					
ark	-Hor	izenta	l									
	hey	ync 🗆	_									
	113					H activ	/e					
		_		×				→'		i		
	d	e										
	u	e –				1	83 clk					
	-Ver	tical										
	VE	inc 🗆						_			<u> </u>	
	VS	/nc			Va	ctive						
			1					-				
		de —		<u> </u>		305	lines	1				
			ľ	<u></u> -				—- > ¦				
estriction												
R40H		DAA/	DICX	D7	De	DE	Bit		02	D1		Code
Inst/Para TSC		R/W W	D/CX 0	D7 0	D6 1	D5 0	D4 0	D3 0	D2 0	D1 0	D0 0	Code 40H
1 st Parame		R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
nd Parame		R	1	D2/ TS[9]	D1/ TS[8]	D0	-	-	-	-	-	-
OTE: "-" De		re, can	be set to	o VDD or	GND level							
escription					as follow							
		This c		d indicat	es the ter	nperatur	e value.	internal te	mporatu		r valuo	
		If R41	H(TSE)	bit7 set	to 1, this	comman	id reads	external (LM75) te	emperatu	re sensor	value
		SP1	TSC			SC neters	-		n 1151	43		
		CSB				[-					
			L	J	L							
		SCL	UUUUUUUU 	L								
						TSC value	-					
		SDA		1	-							
		BUSY_N	5[7:0]/D[10	0:31	T (°C)	TS[7:0]	/D[10:31	T (°C)	TSI7	:0]/D[10:3]	T(°C	2)
		BUSY_N TS	5[7:0]/D[10 1110011	1	T (°C) -25	TS[7:0]/ 0000	0000	T (°C) 0	00	:0]/D[10:3] 0011001	T (°C 25	
		BUSY_N TS		1			0000		00			

	11	a araan ka mit										
		11101001		-23	00000	0010	2	000	11011	27	1	1
		11101001	· · · · · · · · · · · · · · · · · · ·	-23	00000	26.01.00.202	3	5005000,000	11100	28	-	
		11101011		-21	00000		4		11101	29	-	
		11101100)	-20	00000	0101	5	000	11110	30		
		11101101		-19	00000	S	6	11.753	11111	31		
		11101110		-18	00000		7		00000	32		
		11101111		-17	00001		8		00001	33	_	
	-	11110000		-16 -15	00001		9 10		00010 00011	34 35	-	
	-	11110010		-13	00001		10		00100	36	-	
		11110011		-13	00001		12		00101	37	-	
		11110100		-12	00001		13		00110	38	-	
		11110101	l.	-11	00001	1110	14	001	00111	39		
		11110110		-10	00001	2. 3. A. 12	15	10000000	01000	40		
	-	11110111		-9	00010		16		01001	41	_	
	-	11111000		-8 -7	00010		17	2001/00/0	01010	42	-	
	-	11111001	1.	-7 -6	00010		18 19		01011 01100	43	-	
		11111011		-5	00010		20		01100	45	-	
		11111100		-4	00010		21		01110	46	-	
		11111101		-3	00010	0110	22	001	01111	47		
		11111110		-2	00010		23		10000	48		
		11111111	L	-1	00011	1000	24	001	10001	49		
	r	T0(0,0)		200								
		TS[9:8] 00		(°C) +0								
		01	1	.25								
		10		0.5								
		11	+0	.75								
Restriction	This	command	l only act	ives whe	en BUSY_N	J = "1"						-
	1113	command										1
R41H	D 44/					Bit	D 0			D 0		-
Inst/Para TSE	R/W W	D/CX	D7 0	D6	D5 0	D4 0	D3 0	D2	D1	D0	Code	
st Parameter	W	0	0	1 1						1 1	111	
		1	TSE	-	-	TO[4]	TO[3]	0 TO[2]	0 TO[1]	1 TO[0]	41H 00h	
NOTE: "-" Don'i	t care, ca		VDD or		-		2 J					
NOTE: "-" Don't Pescription - 1 F	t care, ca The count This cor Reserve 1. TO[3]	an be set to mmand de nmand ind	<i>VDD or</i> efines as dicates t perature ' or '-' , v	s: he drive offset] while 0 i	e/ er IC tempo [O[3:0] for is '+' ; 1 is	TO[4] erature so calibratio	TO[3]	TO[2]	TO[1]	TO[0]	00h	P
NOTE: "-" Don't Description - 1 F	t care, ca The count This cor Reserve 1. TO[3]	mmand de nmand in one temp : mean '+ 0]: mean	<i>VDD or</i> efines as dicates t perature ' or '-' , v	s: he drive offset] while 0 i	e/ er IC tempo [O[3:0] for is '+' ; 1 is	TO[4] erature so calibratio	TO[3] ensor en	TO[2]	TO[1]	TO[0]	00h	
NOTE: "-" Don't Description - I F	t care, ca The con This cor Reserve 1. TO[3] 2. TO[2:	n be set to mmand de nmand in e one tem : mean '+ 0]: mean Na	VDD or effines as dicates t perature ' or '-' , v tempera me	s: he drive offset] while 0 i iture offs ture offs 0000: 0001: 0100: 0101: 0101: 1000: 1001: 1001: 1001: 1100: 1101: 1100: 1101: 1110:	- el Fo[3:0] for s '+' ; 1 is set value berature lev +0°C (def +0.5°C +1°C +1°C +2.5°C +2.5°C +3°C +3.5°C -3°C -3.5°C -3°C -2.5°C -1°C -1°C -0.5°C	TO[4] erature so calibratio	TO[3] ensor en	TO[2]	TO[1]	TO[0]	00h	
NOTE: "-" Don't Description - I F	t care, ca The co This cor Reserve 1. TO[3] 2. TO[2: Bit	n be set to mmand de nmand in e one tem : mean '+ 0]: mean Na	VDD or efines as dicates t perature ' or '-' , v tempera me	s: he drive offset] while 0 i ture offs ture offs 0000: 0001: 0100: 0101: 0100: 0101: 1000: 1001: 1000: 1001: 1010: 1011: 1100: 1011: 1100: 1111: 1110: 1111: 1110: 1111:	- el er IC tempo [O[3:0] for s '+'; 1 is set value perature lev +0°C (def +0.5°C +1°C +2.5°C +3°C -3°C -3°C -3°C -2.5°C -1.5°C -1.5°C -0.5°C 0°C (defau	TO[4] erature so calibratio '-' vel: ault)	TO[3] ensor en on Desc	TO[2]	TO[1]	TO[0]	00h	

WINSTAR istributed by www.texim-europe.com

Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSW W 0 0 1 0 0 0 0 1 0 1st Parameter W 1 WATTR(7) WATTR(8) WATTR(8) WATTR(9)	Code 42H 00h 00h
Image: style in the ima	00h 00h 00h
2 nd Parameter W 1 WMSB[7] WMSB[6] WMSB[5] WMSB[4] WMSB[3] WMSB[1] WMSB[1] WMSB[0] 3 rd Parameter W 1 WLSB[7] WLSB[6] WLSB[5] WLSB[3] WLSB[2] WLSB[1] WLSB[0] NOTE: *-* Don't care, can be set to VDD or GND level - - The command defines as: This command writes the temperature. 1 * YLSB[7] Pointer setting - - This command writes the temperature. 1 * YLSB[7]	00h 00h
3 rd Parameter W 1 WLSB[7] WLSB[6] WLSB[5] WLSB[4] WLSB[2] WLSB[1] WLSB[0] NOTE: "-" Don't care, can be set to VDD or GND level Description -The command defines as: This command writes the temperature. 1 st Parameter: Bit Name Description 2-0 WATTR[2:0] Pointer setting 5-3 WATTR[2:0] Quere defined address bits (A2, A1, A0) I2-0 WATTR[7:6] QUE WATTR[7:0] Descrip	00h
NOTE: "-" Don't care, can be set to VDD or GND level Description -The command defines as: This command writes the temperature. 1 st Parameter: Bit Name 2-0 WATTR[2:0] Pointer setting 5-3 WATTR[5:3] User-defined address bits (A2, A1, A0) I2C Wite Byte Number 00: 1 byte (head byte only) 7-6 WATTR[7:6] 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer) 11: 4 bytes (head byte + pointer) 11: 4 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer) 11: 4 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer) 7-0 WMSB[7:0] Marameter: Bit <td></td>	
Description -The command defines as: This command writes the temperature. 1 st Parameter: Bit Name 2-0 WATTR[2:0] 5-3 WATTR[5:3] User-defined address bits (A2, A1, A0) I2C Write Byte Number 00: 1 byte (head byte only) 7-6 WATTR[7:6] 01: 2 bytes (head byte + pointer + 1 st parameter) 10: 3 bytes (head byte + pointer + 1 st parameter + 2 nd parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter) 2 nd Parameter: Bit Name Description 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter: Bit Name 0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) Restriction This command only actives after R04H(PON) Restriction This M	<u>er)</u>
This command writes the temperature. 1 st Parameter: Bit Name Description 2-0 WATTR[2:0] Pointer setting 5-3 WATTR[5:3] User-defined address bits (A2, A1, A0) 2-0 WATTR[7:6] U2C Write Byte Number 00: 1 byte (head byte only) 7-6 7-6 WATTR[7:6] 01: 2 bytes (head byte + pointer + 1 st parameter) 10: 3 bytes (head byte + pointer + 1 st parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter 2 nd Parameter: Bit Name Description 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter: Bit Name Description 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) R43H Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 1 0 0 1 <td< td=""><td>ər)</td></td<>	ər)
Bit Name Description 2-0 WATTR[2:0] Pointer setting 5-3 WATTR[5:3] User-defined address bits (A2, A1, A0) 2-0 WATTR[7:6] 12C Write Byte Number 00: 1 byte (head byte only) 7-6 WATTR[7:6] 7-6 WATTR[7:6] 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1 st parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter: Bit Name 2 nd Parameter: Bit Name Description 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter: Bit Name Description 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) R43H Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 1 0 0 0	<u>عامل المحالية المحالي</u>
Bit Name Description 2-0 WATTR[2:0] Pointer setting 5-3 WATTR[5:3] User-defined address bits (A2, A1, A0) 7-6 WATTR[7:6] 12C Write Byte Number 00: 1 byte (head byte only) 7-6 7-6 WATTR[7:6] 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1 st parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter: Bit Name Description 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter: Bit Name Description 7-0 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) R43H Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 1 0 0 0 1 1	er)
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5-3 WATTR[5:3] User-defined address bits (A2, A1, A0) I2C Write Byte Number 00: 1 byte (head byte only) 7-6 WATTR[7:6] 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1 st parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter) 2 nd Parameter: Bit Name 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter: Bit Name 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) Restriction Bit Inst/Para R/W 0 0 0 0 1 Inst/Para W 0 0 0 0 1	er)
I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1 st parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter 2 nd Parameter: Bit Name 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter: Bit Name 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor 3 nd Parameter: Bit Name 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) Restriction This command only actives after R04H(PON) Restriction This command only actives after R04H(PON) Bit Inst/Para W 0 0 1 0 0 0 1 1	ər)
7-6 WATTR[7:6] 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1 st parameter) 11: 4 bytes (head byte + pointer + 1 st parameter) 2 nd Parameter: Bit Name Description 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter: Bit Name Description 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor 3 nd Parameter: Bit Name Description 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) R43H Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 0 1 0 0 0 1 1	er)
10: 3 bytes (head byte + pointer + 1 st parameter) 11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter) 2 nd Parameter: Bit Name 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter: Bit Name 0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 0 1 0 0 0 1 1	er)
11: 4 bytes (head byte + pointer + 1 st parameter + 2 nd parameter 2 nd Parameter: Description 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter: Description 8it Name Description 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) R43H Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 0 1 0 0 0 1 1	er)
Bit Name Description 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter:	
Bit Name Description 7-0 WMSB[7:0] MSByte of write-data to external temperature sensor 3 nd Parameter:	
Bit Name Description Bit Name Description 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 1 0 0 1 1	
Bit Name Description 7-0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) R43H Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 0 1 0 0 0 1 1	
7-0 WLSB[7:0] LSByte of write-data to external temperature sensor Restriction This command only actives after R04H(PON) R43H Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 0 1 0 0 0 1 1	
Restriction This command only actives after R04H(PON) R43H Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 0 1 0 0 0 1 1	
R43H Bit Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 0 1 0 0 0 1 1	
Inst/Para R/W D/CX D7 D6 D5 D4 D3 D2 D1 D0 TSR W 0 0 1 0 0 0 1 1	
TSR W 0 0 1 0 0 0 1 1	
	Code
1 RMSB[7] RMSB[6] RMSB[5] RMSB[4] RMSB[3] RMSB[2] RMSB[1] RMSB[1] RMSB[0]	43H
	-
2 nd Parameter R 1 RLSB[7] RLSB[6] RLSB[5] RLSB[4] RLSB[3] RLSB[2] RLSB[1] RLSB[0]	-
NOTE: "-" Don't care, can be set to VDD or GND level	
Description -The command defines as:	
This command reads the temperature sensed by the temperature sensor.	
1 st Parameter: Bit Name Description	
7-0 RMSB[7:0] MSByte of read-data from external temperature sensor	
2 nd Parameter:	
Bit Name Description	
7-0 RLSB[7:0] LSByte of write-data from external temperature sensor	
SPI	
TSR TSR Command parameters	
CSB	
SCLUUUUUUU	
SDA value	
BUSY_N	
Restriction This command only actives after R04H(PON)	



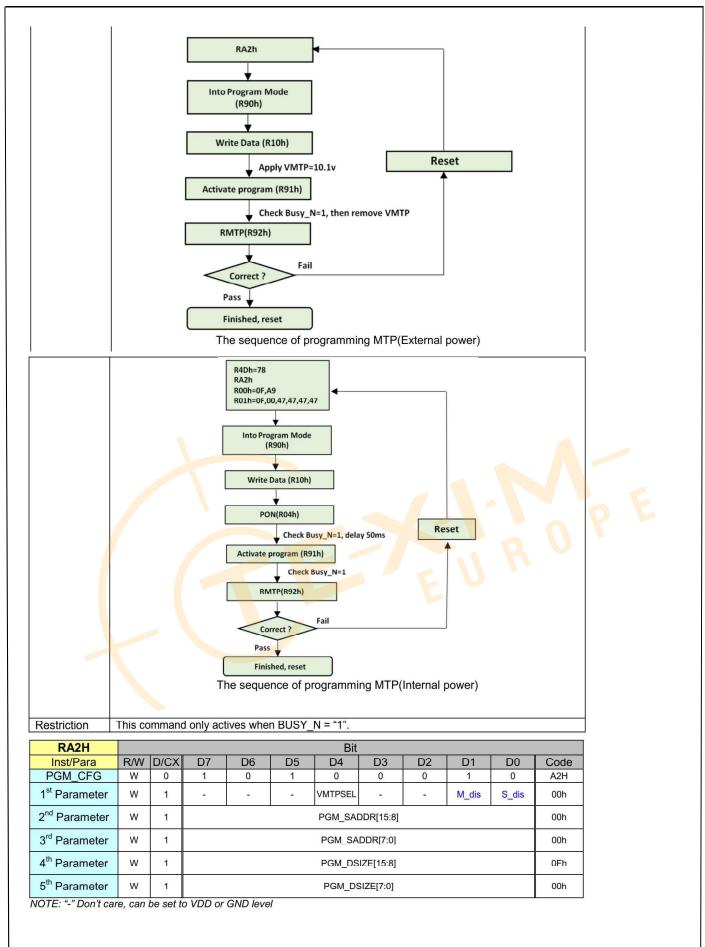
R51H						Bit					
Inst/Para	R/W	D/	CX D	7 D6	5 D5	D4	D3	D2	D1	D0	Code
LPD	W	(0 0	1	0	1	0	0	0	1	51H
1 st Parameter	R		1 -	-	-	-	-	-	-	LPD	
IOTE: "-" Don't ca	are, car	n be se	t to VDD o	r GND leve	el				10		
OTE: "-" Don't ca	-The c This c batter When When 1 st Pa Bit 0 1 C	xomma ommai y's con LPD=' LPD=' ramete 0 SB	nd defines nd indicate dition. '1", systen '0", systen er: Low p	s as: es the inpu n input po	ut power c wer is nor wer is low ut. s.	mal.				n RE4H (L	
	S	DA _							va	lue	
	BUS	SY_N					L				
Restriction	This c	ommai	nd only ac	tives whe	n BUSY_N	N = " <u>1</u> ".					
R61H						Bit					
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1 st Parameter	W	1	-			-		-	HRES(
2 nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3) HRES(2		0	00h
3 th Parameter	W	1	- \	-	-	-	-	-	VRES(S	9) VRES	(8) 00h
4 th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3) VRES(2	2) VRES(1) VRES	(0) 00h
OTE: "-" Don't ca	are, car	1 be se	t to VDD o	r GND leve	el						
Description	When Horiz Vertion Note No m	n using contal o cal dis natter h natter h	and defin g register: display re play resol HRES[9:8 sable calo st G activ	solution(s ution(gate],HRES[1 culation:	source) = e) = VRE :0],VRES	S 5[9:8] valu				e 00b.	
	G	E D: Firs LAS	st active of X :128x28 t G active F active G st active of	50 e = G0 iD= 0+25	0-1= 249;		SD= first	active +H	ires[9:2]	*4-1	
Restriction		LAS	Factive S	D=0+32*	4-1=127;						
		Jondi	resolution	SHOULU D	e 4-muiti						
R65H Inst/Para	R/M	D/CX	D7	D6	D5	D4 Bit	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1 st Parameter	W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h
2 nd Parameter	w	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	0	0	00h
3 rd Parameter	w	1	-				-	-	G_start[9]	G_start[8]	00h
4 th Parameter	w	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h
NOTE: "-" Don't c	care, ca	n be se	t to VDD oi	GND leve	I						

Description Restriction R70H Inst/Para REV 1 st Paramete 2 nd Paramete 3 rd Paramete NOTE: "-" Don't	Note: No ma 1.S_St 2.G_St S_Start R/M r R r R r R r R	tter S_ art [8:0 art[8:0 should v E	_start[§ 0] desc 0] desc 0 d be the 0 1 1 1 1 set to V	cribe wh cribe wh e multiple 0 0 0 0 0 0 0 0 0 0 0	ich sou ich gate e of 4 D6 1 0 0 0 ND level)], G_star rce outpu line is th D5 1 0 0 0	t line is th	ne first da		D1 0 1 0 1 0	be 00b. D0 0 1 0 1 1	Code 70H 09h 02h 01h
Description				efines as								
	1 st &	2 nd & Bit	3 rd Pa	rameter		scription						
		<u>л.</u> 7-0	СНІ	P_REV		scription						
Restriction												
R80H							Bit					
Inst/Para	R/W	D/0		D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV 1 st Parameter	W	1		1 P[1]	0 P[0]	0 AMVT[1]	0 AMVT[0]	0 XON	0 AMVS	0 AMV	0 AMVE	80H 00h
NOTE: "-" Don't							Alviv I [0]	XUN	AIVIV3	AIVIV	AIVIVE	UUII
Description	-The This	comn	nand c nand ir	lefi <mark>n</mark> es a	as:	status. Ho	ost can re	ad this d	lata to un	derstand	d the IC s	tatus.
		Bit		lame					cription			
		0	A	MVE	0: Au 1: Au	E: Auto N uto measu uto measu	ure VCOI ure VCOI	V disable	e (default)		
		1	F	MV	0:Ge 1:Ge	: Analog t Vcom v t Vcom v	alue from alue in ar	nalog sig	nal			
	3	2	А	MVS	0: So (defa		out 0V du	iring Auto	o Measur	e VCON		
		3	,	KON	XON 0: Ga (defa		or all Ga ally scan	te ON of <mark>during A</mark>	AMV uto Meas	ure VCC	OM period	
	5	-4	AM	VT[1:0]	The	5s	me of VC			OM peri	od.	
	7	-6	Ρ	[1:0]	The 00: 2 01: 4 10: 8 11: 1	sensing p t (default) t 6						

		voltage —	20.0									
			Status	of Vcom controll	ed by sensin			arter of sensir	ng time			
	BUS	SY N					-					
							:	T				
					Vcom Se	nsing			l (II			
								4	verage of N p	ooint. N	=2,4,8,16	
50 T. M. T. M. M.												
striction	This co	ommand o	nly activ	es when BL	SY_N =	"1".						
R81H				-		Bit					0= 12	T
st/Para VV	R/W W	D/CX 0	D7 1	D6 0	D5 0	D4 0	D3 0	D2	2 D1		D0 1	Code 81H
arameter			1					-				
	R	1	-	VV[6]	VV[5]	VV[4]	VV[3	3] VV[2	2] VV[IJ	VV[0]	
:: "-" Don't	care, car	n be set to	VDD or	GND level								
cription		mmand o										
	I his co	mmand c	could get	t the VCOM	i value							
	1 st Para											
	Bit	Na	ne	VCOM value			Des	cription				
				VV [6:0]	Voltage	V) VV [6	5:0]	Voltage(V)	VV [6:0) V	oltage(V)	1
				0000000 00	h 0	0011100) 1Ch	-1.4	0111000	38h	-2.8	
		1		0000001 01	h -0.05	001110	1 1Dh	-1.45	0111001	39h	-2.85	
				0000010 02	h -0.1	0011110) 1Eh	-1.5	0111010	3Ah	-2.9	
				0000011 03	h -0.15	001111	1 1Fh	-1.55	0111011	3Bh	-2.95	
				0000100 04	h -0.2	010000) 20h	-1.6	0111100	3Ch	-3	
				0000101 05	h -0.25	010000	1 21h	-1.65	0111101	3Dh	-3.05	
				0000110 06		0100010		-1.7	0111110	-	-3.1	
				0000111 07		010001		-1.75	0111111		-3.15	
				0001000 08		0100100		-1.8	1000000		-3.2	
				0001001 09 0001010 0A		010010		-1.85 -1.9	1000001 4 1000010 4		-3.25 -3.3	
				0001010 0A		010011		-1.9	1000010		-3.35	
				00010110B		010100	-	-1.95	1000100		-3.35	
	6-0	VV[6:0]	000110100		010100	-	-2.05	1000100		-3.45	
				0001110 0E		0101010	-	-2.1	1000110	-	-3.5	
				0001111 0F		010101	-	-2.15	1000111		-3.55	
				0010000 10		0101100		-2.2	1001000		-3.6	
	11			0010001 11	h -0.85	010110	-	-2.25	1001001		-3.65	
				0010010 12		0101110		-2.3	1001010		-3.7	
				0010011 12	h -0.95	010111	-	-2.35	1001011	4Bh	-3.75	
				0010011 13			-	-2.4	1001100	4Ch	-3.8	
				001001113	h -1	011000						
						011000 011000	1 31h	-2.45	1001101 4	4Dh	-3.85	
				0010100 14	h -1.05	-		-2.45 -2.5	1001101 4 1001110 4		-3.85 -3.9	
				0010100 14 0010101 15	h -1.05 h -1.1	011000) 32h	2000.0000		4Eh		
				0010100 14 0010101 15 0010110 16	h -1.05 h -1.1 h -1.15	011000) 32h 1 33h	-2.5	1001110	4Eh 4Fh	-3.9	
				0010100 14 0010101 15 0010110 16 0010111 17	h -1.05 h -1.1 h -1.15 h -1.2	011000 ⁻ 0110010 011001 ⁻) 32h 1 33h) 34h	-2.5 -2.55	1001110 1001111	4Eh 4Fh 50h	-3.9 -3.95	
				0010100 14 0010101 15 0010110 16 0010111 17 0011000 18	h -1.05 h -1.1 h -1.15 h -1.2 h -1.25	011000 0110010 0110011 0110010) 32h 1 33h) 34h 1 35h	-2.5 -2.55 -2.6	1001110 4 1001111 4 1010000 4	4Eh 4Fh 50h	-3.9 -3.95 -4	

R82H						Bit					
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
st Parameter	W	1	-	VDCS[6]	VDCSI5	VDCS [4]	VDCS [3]	VDCS (2)	VDCS [1]		00h
	1919	2880				VDC3 [4]	VDC3 [3]	VDC3 [2]	VDC3[1]	VDC3 [0]	0011
OTE: "-" Don't c	care, can	be set to	VDD or	GND level							
Description	-The co	mmand	defines	as:							
0.8	This co	mmand	set the \	COM DO	C value. D	Driver will	base on	this valu	e for VCN	/_DC.	
	1 st Para	1					_				
	Bit	Na	ame	VCOM va	lue		Descri	otion			
				VDCS [6			6 [6:0] Vo	Itage(V)	/DCS [6:0]	Voltage(V)	î l
				0000000	1 0	ault) 001110			11000 38h	0 ()	
				0000001	,	,			11001 39h		
				0000010	02h -0.	1 00111	10 1Eh	-1.5 01	11010 3Ah	-2.9	1
				0000011	03h -0.1	5 00111	11 1Fh	-1.55 0'	11011 3Bh	-2.95	
				0000100	Approximately of Balan		00 20h		11100 3Ch	1040	
				0000101	Constituente in anotation				11101 3Dh		
				0000110	2.2	S. N. 16 (1999)		2	111110 3Eh	22.00	
				0000111		and an	in vie pointering	Company and a second	111111 3Fh		
				0001000 0001001			00 24h		00000 40h		
				0001001	40.0007	5200	41.15 MICCANORD	1001303	00001 41h	37480/9770	1
				0001010					00010 42h		1
			010.07	0001100	2				00100 44h		1
	6-0	VDC	S[6:0]	0001101	0Dh -0.6	65 010100	01 29h	-2.05 10	00101 45h	-3.45	1
				0001110	0Eh -0.	7 01010 [.]	10 2Ah	-2.1 10	00110 46h	-3.5	
				0001111	Contraction of the second				00111 47h		
				0010000					01000 48h		
				0010001					01001 49h		
				0010010	- A State - Contraction				01010 4Ah 01011 4Bh		
				0010011					01011 4Bh		
				0010100	us supres us		the second s		01100 40h		
				0010110					01110 4Eh		
				0010111	30.000.000	NR 1990 1997 1997 1997 1997 1997 1997 1997	1178 1178 1178 1178 1178 1178 1178 1178		001111 4Fh		
				0011000	18h -1.3	2 011010	00 34h	-2.6 10	100 <mark>00 5</mark> 0h	-4	
				0011001	19h -1.2	25 011010	01 35h	-2.65	other	-4	
				0011010				-2.7			
				0011011	1Bh -1.3	01101	11 3 <mark>7h</mark>	-2.75			
Restriction											
R83H						Bit					
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	0	0	0	1	1	83H
1 st Paramete		1	-	-	-	PTH_ENB	-	-	HRST[9]		00h
2 nd Paramete	erw	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3	HRST[2		-	00h
3 rd Paramete		1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
4 th Paramete		1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3	HRED[2	-	-	00h
5 th Paramete	r W	1	-	-	-	8	-	-	VRST[9]	VRST[8]	00h
		1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2	VRST[1]	VRST[0]	00h
6 th Paramete		1	-	-	-	-	-	-1	VRED[9]		00h
7 th Paramete		2		VRED[6]	VRED[5]	VRED[4]	VRED[3] VRED[2	VRED[1]		00h
7 th Paramete 8 th Paramete	r w	1	VRED[7]	VICED[0]			C		1	PMODE	00h
7 th Paramete 8 th Paramete 9 th Paramete	r w r W	1	-	(a)	2	2	-	-	-	1.0000000000000	
7 th Paramete 8 th Paramete 9 th Paramete	r w r W	1	-	(a)	2	4	-	-	-		
7 th Paramete 8 th Paramete 9 th Paramete	r W r W care, car	1 1 1 be set t	- to VDD or	(a)	-	-	Ξ.	-	-		
7 th Paramete 8 th Paramete 9 th Paramete NOTE: "-" Don't	r W r W care, car	1 1 1 be set t	- to VDD or	GND leve	-		J		-		
7 th Paramete 8 th Paramete 9 th Paramete NOTE: "-" Don't	r w r W care, car	1 1 be set t comma	o VDD or and sets p	GND leve	-		- escriptio		-]
7 th Paramete 8 th Paramete 9 th Paramete NOTE: "-" Don't	r W r W care, car -This	1 1 o be set t comma Name HRST[§	o VDD or nd sets p e 9:2]	GND leve	idow.	D Idress	escriptio	n			
7 th Paramete 8 th Paramete 9 th Paramete NOTE: "-" Don't	r W r W care, car -This	1 1 comma Nam HRST[§ HRED[§	- to VDD or and sets p e 9:2] 9:2]	GND leve	al start ac	D Idress dress. HR	escriptio	n			
7 th Paramete 8 th Paramete 9 th Paramete NOTE: "-" Don't	r W care, car -This	1 1 comma Name HRST[S HRED[S VRST[S	- o VDD or and sets p e 9:2] 9:2] 9:2] 9:0]	GND leve cartial wir Horizonta Horizonta Vertical s	al start ac al end ad	D Idress dress. HR ess.	escriptio	n t be grea	ter than F	IRST.	
7 th Paramete 8 th Paramete 9 th Paramete NOTE: "-" Don't	r W care, car -This	1 1 comma Nam HRST[§ HRED[§	- o VDD or and sets p e 9:2] 9:2] 9:2] 9:0]	GND leve oartial wir Horizonta Horizonta Vertical s Vertical s	al start ac al end ad start addre	D Idress dress. HR ess. ess. VREI	ED mus	n t be grea	ter than F	IRST.	
7 th Paramete 8 th Paramete 9 th Paramete NOTE: "-" Don't	r W care, car -This	1 1 comma Nam HRST[§ VRST[§ VRED[§	- o VDD or nd sets p e 9:2] 9:2] 9:0] 9:0]	GND leve partial wir Horizonta Horizonta Vertical s Vertical e 0: disable	al start ac al end ad start addre end addre e partial r	D Idress dress. HR ess. ess. VREL node(defa	ED mus	n t be grea	ter than F	IRST.	-
7 th Paramete 8 th Paramete 9 th Paramete NOTE: "-" Don't	r W care, car -This	1 1 1 1 1 1 1 1 1 1 1 1 1 1	- o VDD or nd sets p 9:2] 9:2] 9:2] 9:2] 9:2] 9:2] 9:2] 9:2]	GND leve oartial wir Horizonta Horizonta Vertical s Vertical e 0: disable 1: enable	al start ac al end ad start addre end addre e partial r	D Idress dress. HR ess. vREI node(defa node	ED mus D must be ault)	n t be grea e greater	ter than F	IRST.	-
7 th Paramete 8 th Paramete 9 th Paramete NOTE: "-" Don't	r W care, car -This	1 1 comma Nam HRST[§ VRST[§ VRED[§	- o VDD or nd sets p 9:2] 9:2] 9:2] 9:2] 9:2] 9:2] 9:2] 9:2]	GND leve oartial wir Horizonta Horizonta Vertical s Vertical e 0: disable 1: enable 0:Source	al start ac al end ad start addre end addre e partial r output ena	D Idress dress. HR ess. vREI node(defa node able follow	ED mus D must be ault)	n t be grea e greater	ter than F	IRST.	-
7 th Paramete 8 th Paramete 9 th Paramete NOTE: "-" Don't	r W care, car -This	1 1 1 1 1 1 1 1 1 1 1 1 1 1	- o VDD or nd sets p 9:2] 9:2] 9:2] 9:2] 9:2] 9:2] 9:2] 9:2]	GND leve oartial wir Horizonta Horizonta Vertical s Vertical e 0: disable 1: enable 0:Source	al start ac al end ad start addre end addre e partial r	D Idress dress. HR ess. vREI node(defa node able follow	ED mus D must be ault)	n t be grea e greater	ter than F	IRST.	

	alway	n <mark>atter H</mark> ys be 00)b.	,HRST[9:] value	being	filled,	<mark>it's</mark>
	Gate	s scan	both ins	ide and o	outside	of the pa	rtial wind	low.				
				_ENB set					ial wind	ow		
Restriction												
R90H						Bit						
Inst/Para PGM	R/W W	D/CX	D7	D6	D5	D4	D3	D2	D1		D0 0	Code 90H
				1		. ·					0	0011
OTE: "-" Don't o	care, car	n be set t	to VDD or	GND leve	1							
Description	10 10 10 10 10 10 10 10 10 10 10 10 10 1			as follow								
				issued, th				gram m	ode.			
	The m	node wo	uld retur	n to stand	by by ha	ardware r	eset.					
Restriction												
R91H						Bit						
Inst/Para	R/W	D/CX	D7	D6	D5	DIL D4	D3	D2	D1		D0	Code
APG	W	0	1	0	0	1	0	0	0		1	91H
OTE: "-" Don't d	care, car	n be set t	to VDD or	GND leve								
				as follows ransmitte		ogrammi	ng state r	nachine	would	be act	tivated	i.
	After th	iis comn	nand is t	ransmitte	d, the pr	-		1				
Restriction	After th	iis comn	nand is t		d, the pr	0 to 1 wh	nile the pr	1				
Restriction R92H	After th	iis comn JSY flag	nand is t	ransmitte	d, the pr	-	nile the pr	1				
Restriction	After th	iis comn	nand is t	ransmitte	d, the pr	0 to 1 wh	nile the pr	ogramm	ling is c		eted.	
Restriction R92H Inst/Para RMTP	After th	ISY flag	would c	ransmitte hange sta	d, the pr ate from D5	0 to 1 wh Bit D4	nile the pr	ogramm D2	ning is c		eted.	Code
Restriction R92H Inst/Para	After th	JSY flag	would c	ransmitte hange sta	d, the pr ate from D5 0	0 to 1 wh Bit D4	D3 0 nmy	ogramm D2 0	ning is c		eted.	Code 92H
Restriction R92H Inst/Para RMTP 1 st Parameter	After th The BL R/W W R R	JSY flag	would c	ransmitte hange sta	d, the pr ate from D5 0 The dat	0 to 1 wh Bit D4 1 Dur	D3 0 nmy s 0x000 in t	ogramm D2 0	ning is c		eted.	Code 92H
Restriction R92H Inst/Para RMTP 1 st Parameter 2 nd Parameter	After th	JSY flag	would c	ransmitte hange sta	d, the pr ate from D5 0 The dat	0 to 1 wh Bit D4 1 Dur ta of address	D3 0 nmy s 0x000 in t	ogramm D2 0	ning is c		eted.	Code 92H
Restriction R92H Inst/Para RMTP 1 st Parameter 2 nd Parameter 3 rd Parameter 4 th Parameter 5 th Parameter	After the BL R/W W R R R R R	JSY flag	would c	ransmitte hange sta	d, the pr ate from D5 0 The dat	0 to 1 wh Bit D4 1 Dur ta of address	D3 0 nmy s 0x000 in t s 0x001 in t	ogramm D2 0 he MTP he MTP	ning is c		eted.	Code 92H
Restriction R92H Inst/Para RMTP 1 st Parameter 2 nd Parameter 3 rd Parameter 4 th Parameter	After the BL R/W W R R R R R	JSY flag	would c	ransmitte hange sta	d, the pr ate from D5 0 The dat	0 to 1 wh Bit D4 1 Dur ta of address	D3 0 nmy s 0x000 in t s 0x001 in t	ogramm D2 0 he MTP he MTP	ning is c		eted.	Code 92H
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Restriction R92H Inst/Para RMTP 1 st Parameter 2 nd Parameter 3 rd Parameter 4 th Parameter 6 th ~(m-1) th Parameter m th Parameter	After the BL	JSY flag	nand is t	change sta	d, the pr ate from D5 0 The dat The dat The dat	0 to 1 wh Bit D4 1 Dur ta of address ta of address	D3 0 0 0 nmy s s 0x000 in f s 0x000 in f ss (n-1) in f	ogramm D2 0 he MTP he MTP	ning is c		eted.	Code 92H
Restriction R92H Inst/Para RMTP 1 st Parameter 2 nd Parameter 3 rd Parameter 4 th Parameter 5 th Parameter 6 th ~(m-1) th	After the BL	JSY flag	to VDD o	ransmitte	d, the pr ate from D5 0 The dat The dat The dat	0 to 1 wh Bit D4 1 Dur ta of address ta of address	D3 0 0 0 nmy s s 0x000 in f s 0x000 in f ss (n-1) in f	ogramm D2 0 he MTP he MTP	ning is c		eted.	Code 92H
Restriction R92H Inst/Para RMTP 1 st Parameter 2 nd Parameter 3 rd Parameter 4 th Parameter 6 th ~(m-1) th Parameter m th Parameter m th Parameter	After the BL R/W W R R R R R R R R R R R R Care, cal	JSY flag	to VDD or	ransmitte	d, the pr ate from D5 0 The dat The dat The dat The dat	0 to 1 wh Bit D4 1 Dur ta of address ata of address ata of address	D3 0 nmy s 0x000 in t s 0x001 in t s 0x001 in t c ss (n-1) in th ess (n) in th	ogramm D2 0 he MTP he MTP	D1		D0 0	Code 92H - - - - - - - - -
Restriction R92H Inst/Para RMTP 1 st Parameter 2 nd Parameter 3 rd Parameter 4 th Parameter 6 th ~(m-1) th Parameter m th Parameter m th Parameter	After th The BL R/W W R R R R R R R R R R Care, cal The C	JSY flag	to VDD of and defined is use	ransmitte	d, the pr ate from D5 0 The dat The dat The dat The dat The dat dat The dat	0 to 1 wh	nile the pr D3 0 nmy s 0x000 in t s 0x001 in t s 0x001 in t : : : : : : : : : : : : : : : : : : :	ogramm D2 0 he MTP he MTP e MTP	g the da	omple	progra	Code 92H - - - - - - - - amming.
Restriction R92H Inst/Para RMTP 1 st Parameter 2 nd Parameter 3 rd Parameter 4 th Parameter 6 th ~(m-1) th Parameter m th Parameter m th Parameter	After th The BL R/W W R R R R R R R R R R Care, cal The C	JSY flag	to VDD of and defined is use	ransmitte	d, the pr ate from D5 0 The dat The dat The dat The dat The dat dat The dat	0 to 1 wh	nile the pr D3 0 nmy s 0x000 in t s 0x001 in t s 0x001 in t : : : : : : : : : : : : : : : : : : :	ogramm D2 0 he MTP he MTP e MTP	g the da	omple	progra	Code 92H - - - - - - - - amming.



	This comm	and is used		contiguration of M	IP				
	1 st Parame		for setting	configuration of wh					
	Bit	Nam	ne		Description				
	0	S_di	is 0: 1:	slave enable some slave disable some	command (de command				
	1	M_d		master enable som master disable som		default)			
	4	VMTPS		xternal VMTP (def nternal VMTP	ault)				
				and when IC sets s and when IC sets n					
		mand define i), R83H(PTI		rameter 1) (PSR), I	R10H(DTM),	R90H(PG	iΜ),		
	Command	read							
	M_dis	S_dis		Description	t in the second s				
Description	0	0	command	read from master					
Description	0	1	command	read from master					
	1	0		read from slave					
	1	1	command	read from slave					
	Note: If user prog	gram Area0 (2 <mark>E</mark> [15:0] will	(0x00~0x0	d Read MTP start a a size PGM_DSIZE 17F), PGM_SADDF 180.					
		ITP FIOW							
	R4Dh=7/ R01I=0F;0,47, PON(R04 RA2H=01 h o FA2H=01 h o Write data(R Activate program	8 47,47,47 H) IC (11) to (RUOH) 10H)		Set Slave IC XZH-02h or 12h rogram Mode (R90H) white data(R10H) the data(R10H) POFF(R02H) POFF(R02H) cade Finish, Reset			R		PF
Restriction	R4Dh=7/ R01I=0F;0,47, PON(R04 + FA2H=01h o Into Program Moc	8 47,47,47 H) IC (11) to (RUOH) 10H)		Vrite data(R10H)			P		PE
Restriction RE0H Inst/Para	RADh=7/ Roth=or;0,47, PON(R04 FX2H=01h o FX2H=01h o Write data(R Write data(R	8 47,47,47 H) IC (111) 10 (H90H) 10 (H91H) 10 (H91H)		rogram Mode (R90H) Write data(R10H) ate program (R91H) POFF(R02H) cade Finish, Reset Bit D5 D4 E	D3 D2		DO	Code	PE
RE0H Inst/Para CCSET	R4Dh=7/ R01I=0F:0.47, PON(R04 R22H=01h of R22H=01h of	8 47.47,47 H) IC (111) 10(H) 10(H)		rogram Mode (R90H) virte data(R10H) tate program (R91H) POFF(R02H) cade Finish, Reset Bit D5 D4 C 1 0	0 0	0	0	E0H	PE
RE0HInst/ParaCCSETst Parameter	R4Dh-7/ R01I-oF:0.47, PON(R04 Set Master RA2H-OTh o Unto Program Moc	8 47,47,47 H) H) H) He (HOUH) H) He (HOUH) H) H) H) H) H) H) H) H) H) H) H) H) H		rogram Mode (R90H) Write data(R10H) ate program (R91H) POFF(R02H) cade Finish, Reset Bit D5 D4 E			1		PE
RE0H Inst/Para CCSET I st Parameter OTE: "-" Don't car	R4Dh=7/ R01I=0F:0.47, PON(R04 PON(R04 FX2H=01h o Motion Program Moc Wite data(R Write data(R CALIVATE program CALIVATE program C	8 87,47,47 H) H) H) H) H) H) H) H) H) H)		rogram Mode (R90H) Vrite data(R10H) POFF(R02H) Cade Finish, Reset Bit D5 D4 [1 0	0 0	0	0	E0H	PF
RE0H Inst/Para CCSET 1 st Parameter OTE: "-" Don't car	R4Dh-7/ R01I-0F:0.47, PONR04 PONR04 FX2H-01h o FX2H-01h o Write data(R Activate program C R/W D/C W 0 W 1 re, can be set This comman	847.47,47 H) H) H) H) H(HSOH) H(HSOH) H) H(HSOH) H(rogram Mode (R90H) Vrite data(R10H) POFF(R02H) Cade Finish, Reset Bit D5 D4 [1 0	0 0	0	0	E0H	PF
RE0H Inst/Para CCSET 1 st Parameter OTE: "-" Don't car	RADh-7/ RoTI-or.0.47.	87,47,47 H) H) H) H) H(HSO(H) H(HSO(H) H) H(HSO(H) H(HSO(H) H) H(HSO(rogram Mode (R90H) Vrite data(R10H) POFF(R02H) Cade Finish, Reset Bit D5 D4 [1 0	0 0	0	0	E0H	
RE0H Inst/Para CCSET 1 st Parameter OTE: "-" Don't car	RADh-7/ RoTI-or.0.47.	847.47,47 H) H) H) H) H) H) H) H) H) H)	D6 1 - ID level	rogram Mode (R90H) Write data(R10H) tate program (R91H) POFF(R02H) cade Finish, Reset Bit D5 D4 E 1 0 - 	0 0	0	0	E0H	PF
RE0H Inst/Para CCSET 1 st Parameter IOTE: "-" Don't car	RADH-7/ Roth-or.00.47, PON(R04 PON(R04 FX2H-Otho Set Mester FX2H-Otho Write data(R Activate program Activate program C W 0 W 1 re, can be set This comman 1 st Paramete Bit Na	8 7:47,47 H) IC IC	D6 1 - <i>ID level</i> or cascade	rogram Mode (R90H) white data(R10H) popF(R02H) cade Finish, Reset Bit D5 D4 E 1 0 Bit l D6 pos able/disable. de. (default)	0 0	0	0	E0H	
REOH Inst/Para CCSET 1 st Parameter IOTE: "-" Don't car	RADI-7/ RoTI-or.0.47, PON(R04 PON(R04 Wite data(R Write data(R C Write data(R C Write data(R C Write data(R C Write data(R C C C C C C C C C C C C C C C C C C C	87,47,47 H0 11 11 12 13 14 15 15 11 12 13 14 15 15 15 15	D6 1 - <i>ID</i> <i>ID</i> <i>ID</i> <i>ID</i> <i>ID</i> <i>ID</i> <i>ID</i> <i>ID</i>	rogram Mode (R80H) vitte data(R10H) ete program (R91H) poFF(R02H) cade Finish, Reset Bit D5 D4 C 1 0 Desc able/disable. de. (default) node. slave's temperatur value is defined by	0 0 cription re is same as internal temp	0 TSFIX the maste	0 CCEIN er's.	E0H 00h	
RE0H Inst/Para CCSET 1 st Parameter OTE: "-" Don't car	RADI-7/ RoTI-or.0.47, PON(R04 PON(R04 Wite data(R Write data(R C Write data(R C Write data(R C Write data(R C Write data(R C C C C C C C C C C C C C C C C C C C	87,47,47 H0 11 11 12 13 14 15 15 11 12 13 14 15 15 15 15	D6 1 - <i>ID</i> <i>ID</i> <i>ID</i> <i>ID</i> <i>ID</i> <i>ID</i> <i>ID</i> <i>ID</i>	rogram Mode (R80H) write data (R10H) poFF(R02H) cade Finish, Reset Bit D5 D4 C C C D5 D4 C C C C C C C C C C C C C C C C C C	0 0 cription re is same as internal temp	0 TSFIX the maste	0 CCEIN er's.	E0H 00h	

RE3H							Bit					
Inst/Para	R/W	D/CX	D7	D6	D5	D4	9201002200	03	D2	D1	D0	Code
PWS	W	0	1	1	1	0		0	0	1	1	E3H
1 st Parameter	W	1		VCOM_	W[3:0]				SD_W	[3:0]		00h
IOTE: "-" Don't d	care, c	an be s	et to VD	D or GND le	evel						d7.0	
Description	- Thi / Sc will VCC	s comr purce is be acti DM_W: SYNC COM	vated. 7	set for savi egative to p The active power savi OM_W[3:0] CDI[3:0] wer saving	ing powe positive of period w ing width	nit = 500	ositive efined line pe Fram	e to nega by the for eriod) e N VCOM e N data	tive, the	power sa		f VCOM chanism
Restriction RE4H Inst/Para LVSEL st Parameter OTE: "-" Don't content Description		can be s) 1 set to VD		evel	05 I 1 -	Bit 04 -	D3 0 -	D2 1	D1 0 LVD_	D0 0 SEL[1:0]	Code E4H 03h
Restriction		R - R	:0]: Low _SEL[1 00 01 10 11	/ Power Vo :0]	ltage Se	LVD va < 2.2 < 2.3 < 2.4	V V	ault)				
Restriction									_			
					26	D5	Bit D4	D3	D2	D1	D0	Code
RE5H	- P			D7	10	00	D4	100000000	10031/441			
RE5H Inst/Para	R/	CUCHU AND	0/CX	10000000		1	0	0	1	0		E5H
RE5H Inst/Para CCS_sel	V	/	0	D7 [1	1	0	cascade	1	0	1	
RE5H Inst/Para CCS_sel 1 st Parameter	v v	/	0 1	1	1		0			-		E5H 00h
RE5H Inst/Para CCS_sel	v v care, c Thi 1 st	/ / san be s s comr Parame Bit	0 1 <i>bet to VD</i> nand is	1 - D or GND k used for c	1 	-	- SCL / T	cascade_ sync Descript SDA (defa	ion			
RE5H Inst/Para CCS_sel 1 st Parameter IOTE: "-" Don't c	v v care, c Thi 1 st	/ / san be s s comr Parame Bit	0 1 neet to VD nand is eter: Name	1 - D or GND k used for c	1 	-	- SCL / T	cascade_ sync Descript SDA (defa	ion			

8. Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8- 1
CR	Contrast Ratio	Indoor	8:1		-		8-2
T update	Image update time	at 25 °C		26	-	sec	
Life		Topr		1000000times or 5years			

Notes: 8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

9. Handling, Safety and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

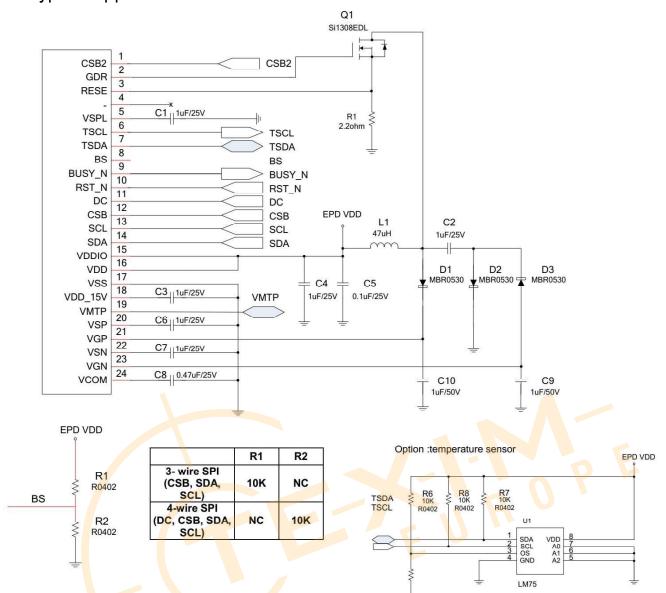
Data sheet status						
Product specification	This data sheet contains final product specifications.					
	Limiting values					
Limiting values given are in accorda	ance with the Absolute Maximum Rating System (IEC					
134).Stress above one or more of th	e limiting values may cause permanent damage to the device.					
These are stress ratings only and op	eration of the device at these or at any other conditions above					
those given in the Characteristics se	ctions of the specification is not implied. Exposure to limiting					
values for extended periods may aff	ect device reliability.					
	Application information					

10. Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60°C, RH=35%, 240h Test in white pattern
3	High-Temperature Operation	T=40°C, RH=35%, 240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=40°C, RH=80%, 240h
6	High Temperature, High Humidity Storage	T=50° C, RH=90%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60°C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m ² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.





Reference table of the device:

De <mark>vic</mark> e no.	Value	Reference
C1,C2,C3, C4, C6, C7, C8	1uF	0603, X5R/X7R, voltage rating : 25V
C9, C10	1uF	0603, X5R/X7R, voltage rating : 50V
C5	0.1uF	0603, X5R/X7R, voltage rating : 25V
R1	2.2Ω	0603, +/-1% variation
		Si1308EDL Si1304BDL
Q1	NMOS	- Drain-source break volatage≧30V
Q	NINOS	- Gate-source threshold voltage≦1.5V
		- Drain-source on-state resistance<400mΩ
		NR4018T470M CDRH2D18/LDNP-470NC
L1	47uH	- Fixed
	4/011	- Maximum DC current~420mA
		- Maximum DC resistance~650mΩ
		MBR0530
54 59	D' 1	- Reverse DC voltage≧30V
D1~D3	Diode	- Forward current≧500mA
		- Forward voltage≦430mV

12. Initialization procedure

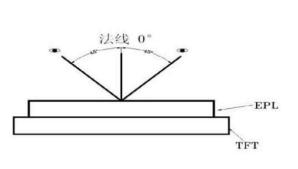
The Initialization procedure is provided with the product.



13. Inspection method and condition

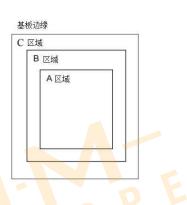
13. 1 Inspection condition

Item	Condition
Illuminance	800~1500 lux
Temperature	$22^{\circ}C \pm 3^{\circ}C$
Humidity	55±10 %RH
Distance	≥30cm
Angle	Vertical fore and aft 45
Inspection method	By eyes



13.2 Zone definition

- A Zone: Active area
- B Zone: Border zone
- C Zone: From B zone edge to panel edge



13. 3 General inspection standards for products

13.3.1 Appearance inspection standard

Inspection item	Figure	A zone inspection standard	B/C zone	Inspection method	MAJ MIN
Spot defects such as dot, foreign matter, air bubble, and dent etc. lefects	Diameter D=(L+W)/2 (L-length, W-width) Measuring method shown in the figure below $L \rightarrow (L+W)/2$ D=(L+W)/2 The distance between the two spots should not be less than 10mm	$\begin{array}{l} \text{7.5"-13.3"Module (Not include} \\ \text{7.5")}: \\ D>1mm \ N=0 0.5 < D \le 0.8 \\ N \le 4 \qquad D \le 0.5 \\ \text{Ignore} 0.8 < D \le 1 \qquad N \le 2 \\ \text{4.2"-7.5"Module (Not include 4.2")}: \\ D>0.5 \ N=0 \qquad 0.4 < D \le 0.5 \\ \text{N} \le 2 \qquad D \le 0.25 \\ \text{Ignore} 0.25 < D \le 0.4 \qquad N \le 4 \\ \text{Module below 4.2":} \\ D>0.5 \ N=0 \qquad 0.4 < D \le 0.5 \\ N \le 1 \\ D \le 0.25 \text{Ignore} 0.25 < D \le 0.4 \\ N \le 4 \\ 0.1mm < D \le 0.25 \qquad N \le 3/\text{cm}^2 \end{array}$	Foreign matter D≤1mm Pass	Check by eyes Film gauge	MIN
Inspection item	Figure	A zone inspection standard	B/C zon	1	MA J/ MI N
Line defects Line defects as scrate hair etc.	hudged by dot	7.5"-13.3"Module (Not include 7.5" t L>10mm,N=0 W>0.8mm, N=0 5mm≤L≤10mm, 0.5mm≤W≤0.8mm N≤2 L≤5mm, W≤0.5mm Module (Not include 4.2") L>8mm,N=0 W>0.2mm, N=2 L>8mm,N=0 W>0.2mm, N=2 Module 4.2") L>8mm,N=0 W>0.2mm, N=2 2mm≤L≤8mm, 0.1mm≤W≤0.2mm L≤2mm, W≤0.1mm Ignore Module below 4.2": L>5mm,N=0 W>0.2mm, N=0 2mm≤L≤5mm, 0.1mm≤W≤0.2mm L≤2mm, W≤0.1mm Ignore	n hore s N≤4 Ignor	Check by eyes Film gauge	MIN

Inspect	Inspection item Figure		Inspection standard	Inspection method	MA J/ MIN
Panel chipping and crack defects	TFT panel chipping	X the length, Y the width, Z the chipping height, T the thickness of the panel M/A Mize	Chipping at the edge: Module over 7.5" (Include 7.5") : $X \le 6mm, Y \le 1mm$ $Z \le T$ N=3 Allowed Module below 7.5"(Not include 7.5"): $X \le 3mm, Y \le 1mm$ $Z \le T$ N=3 Allowed Chipping on the corner: IC sideX $\le 2mm$ Y $\le 2mm$, Non-IC sideX $\le 1mm$ Y $\le 1mm$. Allowed Note: Chipping should not damage the edge wiring. If it does not affect the display, allowed	Check by eyes√ Film gauge	MIN
	Crack	玻璃裂紋	Crack at any zone of glass, Not allowed	Check by eyes Film gauge	MIN
	Burr edge	+,	No exceed the positive and negative deviation of the outline dimensions X+Y≤0.2mm Allowed	Calliper	MIN
	Curl of panel	H Curl height	Curl height H≤Total panel length 1% Allowed	Check by eyes	MIN

WINSTAR Display

Inspect	ion iten	1	Figure	Inspection standard	Inspecti on	MAJ /
PS defect	Water proof film			 Waterproof film damage, wrinkled, open edge, not allowed Exceeding the edge of module(according to the lamination drawing) Not allowed Edge warped exceeds height of technical file, not allowed 	method Check by eyes	MIN
RTV defect	Adhesiv effect	e		Adhesive height exceeds the display surface, not allowed 1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2 .No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3. No adhesive at edge and corner1*1mm, no exposure of wiring, allowed Protection adhesive, coverage width within W≤1.5mm, no break of adhesive, allowed	Check by cycs	MIN
-	Adhesiv re-fill	e		Dispensing is uniform, without obvious concave and breaking, bubbling and swell, not higher than the upper surface of the PS, and the diameter of the adhesive re-filling is not more than 8mm, allowed	Check by eyes	MIN
EC defect	Adhesiv bubble	e	TPT过想参 防水胶涂布区 封边胶边缘 防水胶涂布区 。 Border外缘 (PPL边缘)	 Effective edge sealing area of hot melt products ≥1/2 edge sealing area; Bubble a+b≥1/2 effective width, N≤3, spacing≥5mm, allowed No exposure of wiring, allowed 	Check by eyes	MIN
Insj	pection	tem	Figure	Inspection standard	Inspection method	MAJ MIN
EC defe	ct	lhesive Sect		 Overflow, exceeds the panel side edge, affecting the size, not allowed No adhesive at panel edge≤1mm, mo exposure of wiring, allowed No adhesive at edge and corner 1*1mm, no exposure of wiring, allowed Adhesive height exceeds the display surface, not allowed 	Pisual, caliper	MIN
Silver do adhesive defect	SI	lver dot hesive		 Single silver dot dispensing amount ≥1mm, allowed One of the double silver dot dispensing amount is ≥1mm and the other has adhesive (no reference to 1mm) Allowed 	Visual	MIN
uerect				Silver dot dispensing residue on the panel ≤0.2mm, allowed	Film gauge	MIN
	FF wi	°C ring		FPC, TCP damage / gold finger peroxidation, adhesive residue, not allowed	Visual	MIJ
FPC def		PC lden lger		The height of burr edge of TCP punching surface \geq 0.4mm, not allowed	Caliper	MIN
	FF da ea	mage/cr		Damage and breaking, not allowed Crease does not affect the electrical performance display, allowed C	heck by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Protective film defect	Protective film	Scratch and crease on the surface but no affect to protection function, allowed		Check by eyes	MIN
		Adhesive at edge L≤5mm, W≤0.5mm, N=2, no entering into viewing area		Check by eyes	MIN
Stain defect	Stain	If stain can be normally wiped clean by > 99% alcohol, allowed		Visual	MIN
Pull tab defect	Pull tab	The position and direction meet the document requirements, and ensure that the protective film can be pulled off.		Check by eyes/ Manual pulling	MIN
Shading tape defect	Shading tape	Tilt≤10°, flat without warping, completely covering the IC.		Check by eyes/ Film gauge	MIN
Stiffener	Stiffener	Flat without warping, Exceeding the left and right edges of the FPC is not allowed. Left and right can be less than 0.5mm from FPC edge		Check by eyes	MIN
Label	Label/ Spraying code	The content meets the requirements of the work sheet. The attaching position meets the requirements of the technical documents.		Check by eyes	MIN



14. Packaging

TBD

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