Product Specification

Part Name: Monochrome LCD Graphic Module
Customer Part ID:
Topovision Part ID: TVG12864DAG (FSTN+White LED B/L)
Ver: A

Customer:
Approved by

From: Topovision Technology Co.,Ltd.
Approved by

Notes:

1. Please contact Topovision Technology Co., Ltd. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Topovision Technology Co., Ltd. for any intellectual property claims or other problems that may result from application based on the module described herein.

1. FUNCTIONS & FEATURES

Features

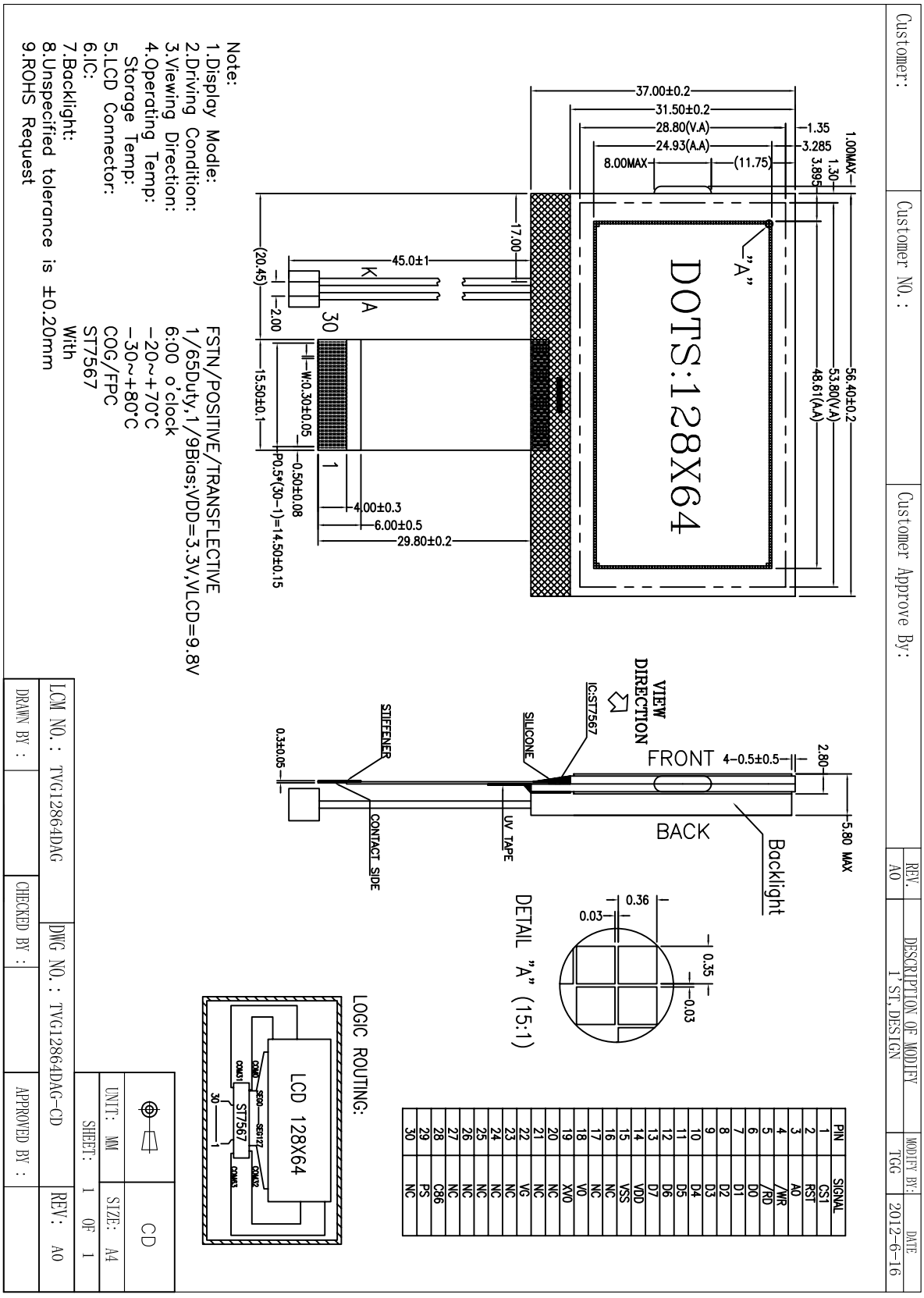
- Dot Matrix: 128×64 Dots
- LCD Mode: FSTN
- Controller IC:ST7567
- Driving Method: 1/64 Duty; 1/9 Bias
- Viewing Angie: 6 O'clock direction
- 8080-series parallel interface
- Operating voltage: 3.3V
- Operating Temperature Range: -20 to +70℃;
- Storage Temperature Range : -30 to +80℃;
- Backlight Speciality : Led(3PCS) Vf=3.0±0.2V，IF=45MA;

Note: Color tone is slightly changed by temperature and driving voltage.

2. MECHANICAL SPECIFICATIONS

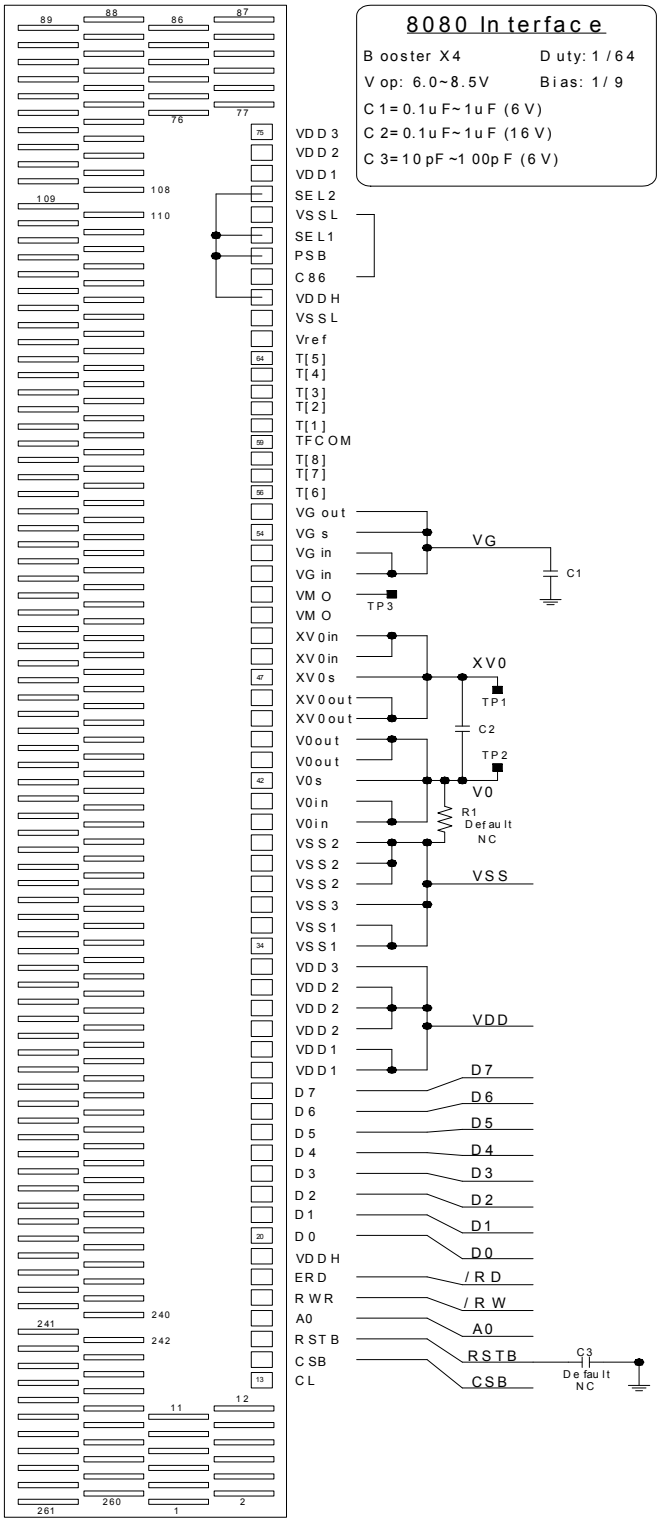
ITEM	SPECIFICATIONS	UNIT
Module Size	56.4L×37.0W×5.4（max）H	mm
View Area	53.8×28.8	mm
Effective Area	128×64	dot
Dot Size	0.35×0.36	mm
Dot Pitch	0.38×0.39	mm

3. EXTERNAL DIMENSIONS

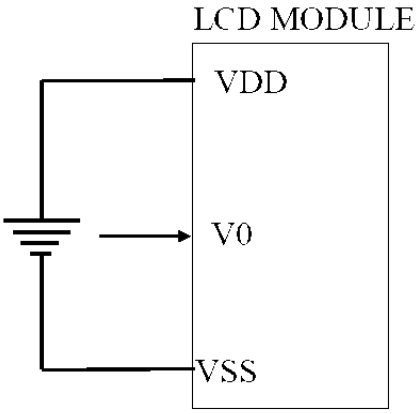


Note: backlight AK length can be customized(背光 AK 线长可定制).

4. BLOCK DIAGRAM



5. POWER SUPPLY



6. PIN DESCRIPTION

ITEM	SYMBOL	LEVEL	FUNCTION
1	CS1	H/L	Chip select input pin. Interface access is enabled when CSB is “L”. When CSB is non-active (CSB=“H”), DB[7:0] pins are high impedance.
2	RST	H/L	Hardware reset input pin. When RSTB is “L”, internal initialization is executed and the internal registers will be initialized.
3	A0	H/L	It determines whether the access is related to data or command. RS=“H” : Indicates that signals on DB[7:0] are display data. RS=“L” : Indicates that signals on DB[7:0] are command.
4	/WR	H/L	Write enable input pin. Signals on DB[7:0] will be latched at the rising edge of WRB signal.
5	/RD	H/L	Read enable input pin. When RDB is “L”, DB[7:0] are in output mode.
6 ~ 13	DB0 ~ DB7	H/L	Data Bus
14	VDD	3.3V	Power Supply For Logic
15	VSS	0V	Power Ground
16~17	NC		
18	V0	--	LCD Power supply voltage
19	XV0	--	LCD Power supply voltage (V0-XV0= -0.3~16V)
20~21	NC		
22	VG		LCD Power supply voltage (-0.3~3.6V)
23 ~27	NC		
28	C86	H/L	C86 selects the microprocessor type in parallel interface mode.
29	PS	H/L	PSB selects the interface type: Serial or Parallel.
30	NC		

7. MAXIMUM ABSOLUTE LIMIT (T=25°C)

Items	Symbol	Standard Value	Unit
Supply Voltage	Vdd	2.4 ～3.6	V
Input Voltage	Vin	Vss～Vdd	V
Operating Temperature	Top	-10～60	℃
Storage Temperature	Tst	-20～70 ℃	

Note: Voltage greater than above may damage the module
All voltages are specified relative to Vss=0V

8. ELECTRICAL CHARACTERISTICS

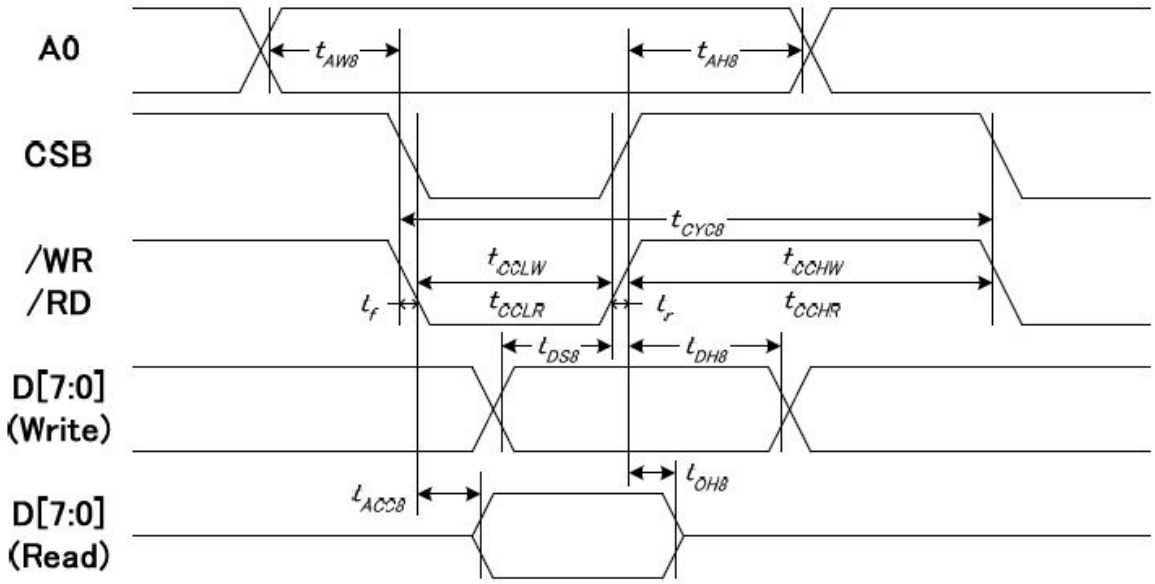
8.1 DC Characteristics (VSS=0V, Ta=-20~+70° C)

Item	Symbol	Condition		Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	VDD1			1.7	—	3.3	V	VDD1
Operating Voltage (2)	VDD2			2.4	—	3.3	V	VDD2
Operating Voltage (3)	VDD3			2.4	—	3.3	V	VDD3
Input High-level Voltage	V_{IHC}			0.7 x VDD1	—	VDD1	V	MPU Interface
Input Low-level Voltage	V_{ILC}			VSS1	—	0.3 x VDD1	V	MPU Interface
Output High-level Voltage	V_{OHC}	I_{OUT}=1mA, VDD1=1.8V		0.8 x VDD1	—	VDD1	V	D[7:0]
Output Low-level Voltage	V_{OLC}	I_{OUT}=-1mA, VDD1=1.8V		VSS1	—	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}			-1.0	—	1.0	μA	MPU Interface
Output Leakage Current	I_{LO}			-3.0	—	3.0	μA	MPU Interface
Liquid Crystal Driver ON Resistance	R_{ON}	Ta=25°C	Vop=8.5V, △V=0.85V	—	0.6	0.8	KΩ	COMx
			VG=1.9V, △V=0.19V	—	1.3	1.5	KΩ	SEGx
Frame Frequency	FR	Duty=1/65, Vop=8.5V Ta = 25℃		70	75	80	Hz	

Note:

The Current Consumption is DC characteristics

8.2 System Bus Timing for 8080 Series MPU



*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast,
(tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.
*2 All timing is specified using 20% and 80% of VDD1 as the reference.
*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

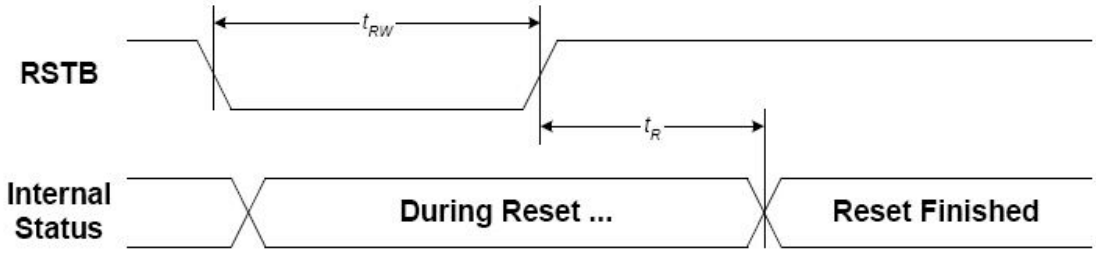
(VDD1 = 3.3V , Ta =25°C)

Item Signal		Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	-	ns
Address hold time		tAH8		10	-	
System cycle time	/WR	tCYC8		240	-	
/WR L pulse width (WRITE)		tCCLW		80	-	
/WR H pulse width (WRITE)		tCCHW		80	-	
/RD L pulse width (READ)	RD	tCCLR		140	-	
/RD H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D[7:0]	tDS8		40	-	
WRITE Data hold time		tDH8		20	-	
READ access time		tACC8	CL = 16 pF	-	70	
READ Output disable time		tOH8	CL = 16 pF	5	50	

(VDD1 = 2.8V , Ta =25°C)

Item Signal		Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	-	ns
Address hold time		tAH8		0	-	
System cycle time	/WR	tCYC8		400	-	
/WR L pulse width (WRITE)		tCCLW		220	-	
/WR H pulse width (WRITE)		tCCHW		180	-	
/RD L pulse width (READ)	RD	tCCLR		220	-	
/RD H pulse width (READ)		tCCHR		180	-	
WRITE Data setup time	D[7:0]	tDS8		40	-	
WRITE Data hold time		tDH8		20	-	
READ access time		tACC8	CL = 16 pF	-	140	
READ Output disable time		tOH8	CL = 16 pF	10	100	

8.3 Handware Reset Timing



(VDD1 = 3.3V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1.0	us
Reset "L" pulse width	tRW		1.0	—	

(VDD1 = 2.8V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	2.0	us
Reset "L" pulse width	tRW		2.0	—	

(VDD1 = 1.8V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	3.0	us
Reset "L" pulse width	tRW		3.0	—	

8.4 INSTRUCTION TABLE

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
(2) Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
(3) Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
(4) Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
(5) Read Status	0	1	0	MX	D	RST	0	0	0	0	Read IC Status
(6) Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
(7) Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
(8) SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
(9) Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
(10) All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
(11) Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
(12) Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
(13) END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
(14) RESET	0	0	1	1	1	0	0	0	1	0	Software reset
(15) COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
(16) Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
(17) Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
(18) Set EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
	0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
(19) Set Booster	0	0	1	1	1	1	1	0	0	0	Double command!! Set booster level: BL=0: 4X BL=1: 5X
	0	0	0	0	0	0	0	0	0	BL	
(20) Power Save	0	0	Compound Command								Display OFF + All Pixel ON
(21) NOP	0	0	1	1	1	0	0	0	1	1	No operation
(22) Test	0	0	1	1	1	1	1	1	1	-	Do NOT use. Reserved for testing.

Note: Symbol "-" means this bit can be "H" or "L".

NOTE:

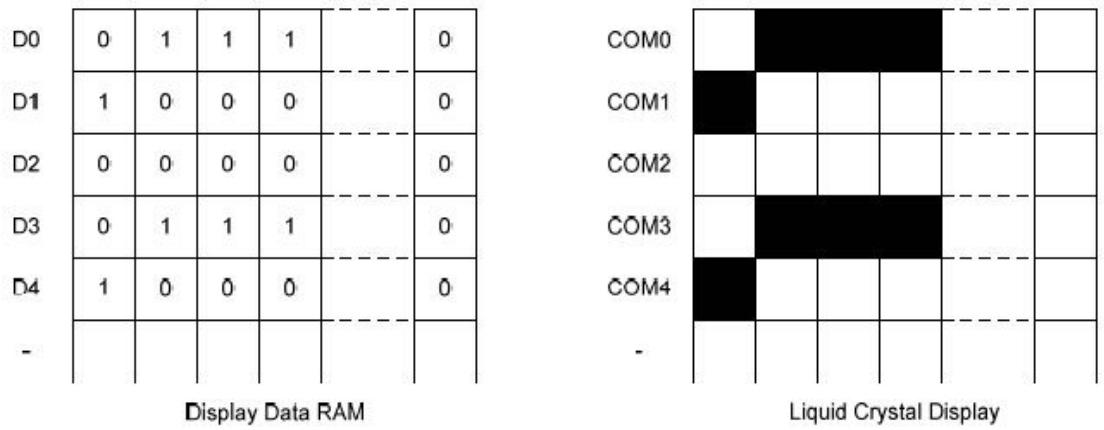
- Do not use any other commands not listed, or the system malfunction may result.
- For the details of rte display commands, please refer to ST7567 datasheet.

9. Display Data RAM(DDRAM)

ST7567 is built-in a RAM with 65X132 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the LCD. It is an addressable array with 132 columns by 65 rows (8-page with 8-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified.

The rows are divided into: 8 pages (Page-0 ~ Page-7) each with 8 lines (for COM0~63) and Page-8 with only 1 line (COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly except icon page. Icon RAM uses only 1-bit of data bus (D0).

The microprocessor can write to and read from (only Parallel interfaces) DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.



Addressing

Data is downloaded into the Display Data RAM matrix in ST7567 as byte-format. The Display Data RAM has a matrix of 65 by 132 bits. The address ranges are: X=0~131 (column address), Y=0~8 (page address). Addresses outside these ranges are not allowed.

Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates 4-bit Page Address Register which can be modified by the “Page Address Set” instruction only. The Page Address must be set before accessing DDRAM content. Page Address “8” is a special RAM area for the icons with only one valid bit: D0.

Column Address Circuit

The column address of DDRAM is specified by the Column Address Set command. The column address is increased (+1) after each display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address “83h”) because the Column Address and Page Address circuits are independent. For example, both Page Address and Column Address should be assigned for changing the DDRAM pointer from (Page-0, Column-83h) to (Page-1, Column-0).

Please refer to ST7567 datasheet.

10. DESIGN AND HANDING PRECAUTION

10.1. The LCD panel is made by glass. Any mechanical shock (eg. Dropping form high place) will damage the LCD module. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.

10.2. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.

10.3. Never attempt to disassemble or rework the LCD module.

10.4. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.

10.5. When mounting the LCD module, make sure that it is free form twisting, warping and distortion.

10.6. Ensure to provide enough space(with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result

10.7. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.

10.8. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.

10.9. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.

10.10. When peeling of the protective film form LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.

10.11. Take care and prevent get hurt by the LCD panel edge.

10.12. Never operate the LCD module exceed the absolute maximum ratings.

10.13. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.

10.14. Never apply signal to the LCD module without power supply.

10.15. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.

10.16. LCD module reliability may be reduced by temperature shock.

10.17. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module