24 DIGITAL I/O WITH COS IRQS FOR MINI PCI EXPRESS HARDWARE MANUAL

MODELS

MPCIE-DIO-24S AND MPCIE-DIO-24



CHAPTER 1: QUICK START

It is recommended that you install the software package before installing the PCI Express Mini Card (mPCle) in your computer. You can install the software¹ using either a stand-alone installer downloaded from the website or an optional Software Master CD.

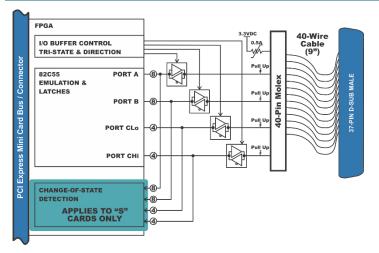
Run the installer you downloaded (or autorun.exe on the Software Master CD) and follow the prompts to install the software for your device.

Please note: during the installation you may be prompted regarding the installation of non-WHQL-certified drivers; please carefully confirm the digitally signed source of the drivers and accept the installation.

Once the software has been installed, shut down your system and carefully install the mPCIe card.

Re-start your system. Once the computer finishes booting, your new digital I/O should already be installed and ready for use; you can confirm this by launching Device Manager and looking under the "Data Acquisition" section. If, for any reason, the device displays a warning triangle, right-click and select "Update Driver".

CHAPTER 2: INTRODUCTION



PCI Express Mini Card (mPCle), a low-profile small-footprint bus standard originally intended for adding peripherals to notebook computers, has become the de-facto standard for high-performance, small form-factor devices in many applications.

- PCI Express Mini Card (mPCle) type F1, with latching I/O connector
- 24 high-current DIO lines (24mA source/sink)
- Change-of-State (CoS) detection IRQ generation
- 2x 8-bit and 2x 4-bit ports, independently selectable for inputs or outputs
- All signals brought out to an optional panel-mountable 37-pin male D-sub connector
- RoHS ships as standard

The advanced logic circuit supports a wide variety of features in addition to simple digital control or monitoring, and additional features can be created, just for you!

The mPCIe-DIO-24S retains backward compatibility with both the PCI and PCIe models, but introduces a wide array of alternate features, fully leveraging the power of the onboard FPGA.

CHAPTER 3: HARDWARE

This manual applies to the following models:

mPCle-DIO-24S 24 Digital I/O w/CoS IRQ mPCle Card mPCle-DIO-24 24 Digital I/O mPCle Card

These models are full-length "F1" mPCIe devices (30×50.95 mm). All units are RoHS compliant.

INCLUDED IN YOUR PACKAGE

mPCle-DIO card Printed QuickStart Guide

Available accessories include:

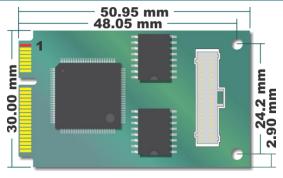
CAB-mPCle-DB37M DB37 cable accessory

ADAP37, STA-37 37-pin Screw Terminal Accessories mPCle-HDW-KIT2 Mounting hardware for 2mm mPCle-HDW-KIT2.5 Mounting hardware for 2.5mm

Contact the factory for information regarding additional accessories, options, and specials that may be available to best fit your specific

application requirements, such as Industrial Temp (-40°C to 85°C).

CHAPTER 4: CONFIGURATION SETTINGS



All configuration of this device is performed through software; there are no jumpers or switches to set.

CHAPTER 5: PC INTERFACE

This product interfaces with a PC using a PCI Express Mini Card (mPCle) connection; a small-form-factor, high-performance, rugged peripheral interconnect technology first introduced for use in laptops and other portable computers.

mPCIe's small size and powerful performance, combined with perfect software compatibility with PCI and PCIe peripheral designs, have led to its recent adoption as a go-to standard for embedded Data Acquisition and Control, and many other applications.

Although mPCle is a broadly-adopted industry standard, the actual connection to the computer shares a specification with mSATA: both mSATA and mPCle use the same edge-connector. In fact, well-designed PCs can automatically detect and configure their onboard connectors to work with either mPCle or mSATA devices – and, according to the standards for mPCle and mSATA they are *supposed* to do so! However, some PC manufacturers ship computers that *only* support mSATA devices. Please confirm in your PC

¹ In Linux or OSX please refer to the instructions in those directories.

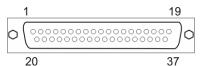
documentation that your edge-connector is *actually* PCI Express Mini Card compliant before installing this, or any, mPCIe card. Damage might occur if you install an mPCIe device into a computer that only supports mSATA.

mPCIe defines mounting holes for securing the otherwise loose end of the card, so it is impossible for these cards to wiggle or flap themselves loose (which was a recurring problem with the older PCI Mini devices). Eliminating this concern for PCI Express Mini Cards is a major reason this standard has seen rapid adoption by the Data Acquisition and Control industry. Unfortunately, a variety of mounting standoff lengths exist; ACCES offers stand-off kits in both 2mm and 2.5mm sizes. Some computers may provide stand-offs. Please consult your computer manufacturer if it requires a different size.

The mPCIe standard, like its PCI Mini Card predecessor, was designed assuming use primarily in Laptop or Notebook and similar devices, where physical dimension is often the paramount design constraint. In Data Acquisition and Control applications low-weight and vibration tolerance tend to be of more concern.

CHAPTER 6: I/O INTERFACE

Most customers will use the optional CAB-mPCle-DB37M's D-Sub Miniature 37-pin Male connector.



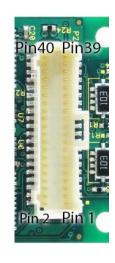
CAB-mPCle-DB37	7M I	Male	37-Pin Pinout
Assignment	P	in	Assignment
Ground	1	20	*Fused +3.3VDC
No Connect	2	21	*Ground
DIO Port CHi bit 7	3	22	DIO Port B bit 7
DIO Port CHi bit 6	4	23	DIO Port B bit 6
DIO Port CHi bit 5	5	24	DIO Port B bit 5
DIO Port CHi bit 4	6	25	DIO Port B bit 4
DIO Port CLo bit 3	7	26	DIO Port B bit 3
DIO Port CLo bit 2	8	27	DIO Port B bit 2
DIO Port CLo bit 1	9	28	DIO Port B bit 1
DIO Port CLo bit 0	10	29	DIO Port B bit 0
No Connect	11	30	DIO Port A bit 7
No Connect	12	31	DIO Port A bit 6
No Connect	13	32	DIO Port A bit 5
No Connect	14	33	DIO Port A bit 4
No Connect	15	34	DIO Port A bit 3
*Fused +3.3VDC	16	35	DIO Port A bit 2
*Fused +3.3VDC	17	36	DIO Port A bit 1
*Ground	18	37	DIO Port A bit 0
*Ground	19		

Notes: Pin 20 is connected to 16 & 17.

*Fused +3.3VDC signals are outputs from the mPCle bus with standard card version. If TTL Factory Option is ordered, these become User VCCIO inputs which can be 4.5VDC to 5VDC.

For customers needing deeper integration the on-card connector is a 40-pin latching Molex 501190-4017 connector. The mating connector is the Molex 501189-4010.

40-Pin latching w	/ire-	to-bc	oard connector
Assignment	Р	in	Assignment
Fused +3.3VDC	40	39	DIO Port C bit 3
Fused +3.3VDC	38	37	DIO Port C bit 2
Fused +3.3VDC	36	35	DIO Port C bit 1
Fused +3.3VDC	34	33	DIO Port C bit 0
Ground	32	31	DIO Port B bit 7
Ground	30	29	DIO Port B bit 6
Ground	28	27	DIO Port B bit 5
Ground	26	25	DIO Port B bit 4
Factory Use Only	24	23	DIO Port B bit 3
Factory Use Only	22	21	DIO Port B bit 2
Factory Use Only	20	19	DIO Port B bit 1
Factory Use Only	18	17	DIO Port B bit 0
Factory Use Only	16	15	DIO Port A bit 7
Factory Use Only	14	13	DIO Port A bit 6
Factory Use Only	12	11	DIO Port A bit 5
Factory Use Only	10	9	DIO Port A bit 4
DIO Port C bit 7	8	7	DIO Port A bit 3
DIO Port C bit 6	6	5	DIO Port A bit 2
DIO Port C bit 5	4	3	DIO Port A bit 1
DIO Port C bit 4	2	1	DIO Port A bit 0



Alternately, custom hardware cables and/or interfaces can be produced to fit your specific application requirement.

CHAPTER 7: SOFTWARE INTERFACE

The simplest way to program for the device is using legacy-compatibility mode: the device boots into this mode, and you can control it exactly like you would a PCIe-DIO-24S. In this mode the unit provides I/O-mapped registers: 4 DIO registers, basically compatible with the 82C55 Mode 0, and several control registers. Note several functions are duplicated for compatibility with a broader range of existing software and devices.

	I/O	Registers at BAR [2]			
	Register [hex]	Write Operation	Read Operation		
8	Port A [+ 0]	Bits 0-7 output	Bits 0-7 input		
2	Port B [+ 1]	Bits 8-15 output	Bits 8-15 input		
5	Port CHi & CLo [+2]	Bits 16-23 output	Bits 16-23 input		
5	Control [+3]	Per-Port Direction	Control		
	[+4+9]	unused			
D	IO Buffer Control [+ A]	Control DIO Buffer	Control DIO Buffer direction / enable		
	CoS Mask [+ B]	Per-Port Change-of-State Enable			
	[+C]	unused			
G	lobal IRQ Disable [+ D]	Write anything to disable all IRQ			
G	ional ind disable [+ D]	sources			
	C3 IRQ Enable [+ E]	En- / Dis-able C3	C3 IRQ Enable Status		
	IRQ Clear [+ F]	Clear IRQ	unused		
	IRQ Control [+ 28]	En- / Dis-able C3	unused		
I	RQ Clear/Status [+ 29]	Clear IRQ IRQ Status			
	Note: Registers marked	l with a grey backgr	ound are deprecated.		

Note: Writes to inputs are ignored. Reads of ports configured as output, and of control registers, read-back the value last written

Certain registers are deprecated: they are provided to enable broad compatibility with previous software / hardware, but new software is encouraged to use modern equivalents.

BAR[2]	BIT	D7	D6	D5	D4	D3	D2	D1	D0
Port A	Pin ¹	30	31	32	33	34	35	36	37
[+0]	Bit ²	7	6	5	4	3	2	1	0
Port B	Pin	22	23	24	25	26	27	28	29
[+1]	Bit	15	14	13	12	11	10	9	8
Port CHi	Pin	3	4	5	6				
[+2]	Bit	23	22	21	20				
Port CLo	Pin					7	8	9	10
[+2]	Bit					19	18	17	16
Control	Note: Mode	1 ³	0	0	Α	CHi	0	В	CLo
[+3]	0 only	A, B, 0	CHi, CLo	direct	ion bits	: 1 for ir	nput, 0 f	or outp	ut.
Buffer		0	0	0	0	0	0	0	Dis
[+A]	Set bit D0 to 1 to disable DIO buffers; 0 to enable								
CoS	value	1	1	1	1	1	С	В	Α
Mask [+B]	A, B, CHi	, CLo Co	S IRQ l	oits: 1 fo	or Mask	ced, 0 fc	r Enable	ed	

+ E		D7	D6	D5	D4	D3	D2	D1	D0
C3 IRQ	Wr								C3 En

Setting Bit D0 to 1 enables Port CLo's 3rd bit (pin 7 of the DB37M) rising edges to generate IRQs. Clearing Bit D0 to 0 disables these IRQs.

+ F		D7	D6	D5	D4	D3	D2	D1	D0
Clear	W								0

Writing any value to +F clears all pending IRQ source latches.

+ 28	Dir	D7	D6	D5	D4	D3	D2	D1	D0
IRQ En	W	C3 IR	Q ENAE	BLE					

Writing "FF" will enable rising-edge IRQs on Port C bit 3 (pin 7 of the DB37M). Write 00 to disable.

+ 29	Dir	D7	D6	D5	D4	D3	D2	D1	D0
IRQ Clr	W	Write	0xFF t	o clear	pendi	ng IRQ	S		
IRQ Stat	R								INT

Write "1" to each IRQ status bit to clear the pending IRQ. Bits D1 through D7 are reserved, for best results write "1" to all bits (0xFF).

Reading will give the current IRQ latch state. Bit D0 "1" means "an IRQ was generated".

¹ Pin refers to the pin number at the DSub37 Male connector on the optional CAB-mPCIe-DB37M cable accessory.

In addition to the I/O registers at BAR[2], BAR[0] contains two additional registers.

One register for compatibility with the PCIe product line: Register +0x69 contains a read-only status bit [d7] which indicates the card is generating an IRQ when set [1], and is not generating an IRQ when clear [0].

And, one register for flexibility: 0xFC contains a read-only 32-bit value that indicates which Isolation Module is attached to the base mPCle board. This register is used by our Windows driver to install a child-device which your code will interface with. In other operating systems it may be necessary to query this register in your application code. The following values are defined as of this writing:

0x00000000: No Isolation Module detected (DIO-24 mode)

0x00000001: IDIO-8 Module detected 0x00000002: IIRO-8 Module detected 0x00000003: IDIO-4 Module detected 0x00000004: IIRO-4 Module detected 0x00000005: II-16 Module detected

In addition to the I/O registers at BAR[2], BAR[0] contains one register for compatibility with the PCIe-DIO-24S: Register 0x69 contains a read-only status bit [d7] which indicates the card is generating an IRQ when set [1], and, when clear [0], is not generating an IRQ.

All of these registers can be operated from any operating system using any programming language, using either no driver at all (kernel mode, Linux ioperm(3), DOS, etc.) or using one of the ACCES provided drivers (AlOWDM [for Windows], APCI or AlOComedi [for Linux & OSX]), or using any 3rd party APIs such as provided with Real-Time OSes.

In Windows⁴, please consult the various samples (C#, Delphi, VC6, VB6, and more) to explore how to program the device. The Software Reference Manual.pdf provides reference material covering all AIOWDM driver APIs, and tips for simplifying tasks such as Plug-and-Play card detection. Please note that the Software Reference Manual.pdf will include numerous functions that don't apply to this device. A quick reference of the most-applicable functions is provided, below:

AIOWDM API Quick Reference, DIO w/CoS IRQs					
Function name	Function Purpose				
RelInPortL()	Read 32-bits of data				
RelOutPortB()	Write 8-bits of data				
GetNumCards()	Determine how many cards AIOWDM has				
de civalica a d d	detected in the system				
	Block the thread until the device reports a				
COSWaitForIRQ()	change-of-state has occurred on a pin of an				
COSWATE OF TRQ()	enabled I/O group (or the wait is aborted).				
	Note: only applies to the mPCle-DIO-24S.				

There are quite a few additional entry points provided by AIOWDM.dll; please consult the Software Reference Manual.pdf, and/or the sample programs, for more information.

² Bit refers to both the sequential, logical bit index of the bit (relative to the device' capabilities), and also to the bit index relative to a 32-bit register access of the Port A [+0]. If this device provided 48 bits of DIO, the two numbers would be different: the sequential, logical bit index of Group 1 Port A0 would be "24", while the 32-bit register bit index would be "0".

 $^{^3}$ This bit is a read/write scratchpad. For maximum compatibility with the 8255, always set this bit (to 1).

⁴ In Linux or OSX please refer to the documentation at github.com/accesio/AIOComedi.

Under certain circumstances the following information might prove useful:

PCI Express Mini Card Plug-and-Play Data					
Vendor / Device ID	Card Type				
0x494F / 0x0E57	mPCle-DIO-24S				
0x494F / 0x0C57	mPCle-DIO-24				

PCI Express Mini Card Plug-and-Play Data					
BAR[n]	Description				
0	PCI-DIO-24S compatibility				
1	Advanced Memory Register Set				
2	I/O Register Set [see above]				

A NOTE ABOUT PERFORMANCE

The PCI Express bus and the PCI Express Mini Card standard are capable of very high bandwidth, but the latency per-transaction is roughly the same as all the other busses — it hasn't improved in decades. This means you can expect to usually see a not-less-than 1MHz transaction rate. Typical rates exceed 3MHz $[0.3\mu s]$.

Unfortunately, modern Operating Systems have introduced a new source of latency, the kernel / userland division. Application code runs in userland, which must transition to the kernel in order to perform any hardware operation. This transition adds quite a lot of latency, which varies between different OSes, motherboards and revisions thereof, etcetera. A Windows XP system can see an additional $7\mu s$ per transaction; a modern computer might see $3\mu s$ or less. Any transaction from the kernel itself, however, avoids this additional overhead.

Real-time operating systems will enable the highest transaction rates possible, all the way up to the hardware limits.

The latest information can always be found on the product page on the website. Here are some useful links:

Links to useful downloads					
ACCES web site	http://acces.io				
Product web page	acces.io/mPCle-DIO-24S				
This manual	acces.io/MANUALS/mPCle-DIO-24S.pdf				
Install Package	acces.io/files/packages/mPCle-DIO-24S				
	<u>Install.exe</u>				
Linux / OSX	github.com/accesio/AIOComedi				

CHAPTER 8: SPECIFICATIONS

PCI Express Mini Card Type F1 "Full Length" V1.2 Digital Input / Output Interface Digital Bits 24 Compatibility Performance 1 μs per 32-bit transaction max ~3.5μs in Windows Digital Inputs Logic High Logic Low 0V to 0.8V Digital Outputs (Standard Version) Logic Low Power Output TTL w/user VCCIO Digital Outputs (Logic High Logic Low Digital Outputs (Standard Version) TTL w/user VCCIO Logic Low Digital Outputs Logic High Logic Low Digital Outputs Logic Low Digital Outputs Logic Low Digital Outputs Logic High Support	PC Interfa	ce	
Digital Bits 24 Compatibility 8255 Mode 0 Performance 1 μs per 32-bit transaction max ~3.5μs in Windows Digital Inputs Logic High 2.0V to VCCIO (3.3VDC, 5VDC tolerant) Logic Low 0V to 0.8V Digital Outputs (Standard Version) Logic High 2.0V (min) 24mA source Logic Low 0.55V (max) 24mA sink Power Output +3.3 VDC via 0.5A polyfuse (resetting) TTL w/user VCCIO Digital Outputs 1.65V to 5.5V At DB37M, via polyfuse Logic High 3.8V (min) 32mA UVCCIO = 4.5V	PCI Express Mini Card		Type F1 "Full Length" V1.2
	Digital Inp	ut / Output	Interface
Performance 1 μs per 32-bit transaction max ~3.5μs in Windows Digital Inputs Logic High Logic Low 0V to VCCIO (3.3VDC, 5VDC tolerant) Logic Low 0V to 0.8V Digital Outputs (Standard Version) Logic High Logic Low 0.55V (max) 24mA source Logic Low 9.55V (max) 24mA sink 9.00 Power Output +3.3 VDC via 0.5A polyfuse (resetting) TTL w/user VCCIO Digital Outputs 1.65V to 5.5V At DB37M, via polyfuse Logic High 3.8V (min) 32mA UVCCIO = 4.5V	Digital Bits		24
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Digital Inputs Logic High Logic Low 2.0V to VCCIO (3.3VDC, 5VDC tolerant) Digital Outputs (Standard Version) Logic High Logic Low Digital Outputs Logic Low Power Output Hand Sink Power Output	Performance		1 μs per 32-bit transaction max
Logic Low OV to 0.8V Digital Outputs (Standard Version) Logic High 2.0V (min) 24mA source Logic Low 0.55V (max) 24mA sink Power Output +3.3 VDC via 0.5A polyfuse (resetting) TTL w/user VCCIO 1.65V to 5.5V At DB37M, via polyfuse Digital Outputs Logic High 3.8V (min) 32mA UVCCIO = 4.5V			~3.5µs in Windows
Digital Outputs (Standard Version) Logic High Logic Low Digital Outputs Logic Low Power Output Logic Low Power Output Logic High Logic Low Logic High Logic High Logic Low Low Logic Low Logic Low Logic Low Logic Low Logic Low Logic Low Low Logic Low Low Logic Low Logic Low Logic Low Logic Low Logic Low Logic Low Low Logic Low Logic Low Logic Low Logic Low Logic Low Logic Low Low	Digital Inputs	Logic High	2.0V to VCCIO (3.3VDC, 5VDC tolerant)
(Standard Version) Logic Low 0.55V (max) 24mA sink Power Output +3.3 VDC via 0.5A polyfuse (resetting) TTL w/user VCCIO Digital Outputs Logic High 3.8V (min) 32mA UVCCIO = 4.5V		Logic Low	0V to 0.8V
Power Output +3.3 VDC via 0.5A polyfuse (resetting) TTL w/user VCCIO 1.65V to 5.5V At DB37M, via polyfuse Logic High 3.8V (min) 32mA UVCCIO = 4.5V	Digital Outputs	Logic High	2.0V (min) 24mA source
TTL w/user VCCIO Digital Outputs 1.65V to 5.5V At DB37M, via polyfuse Logic High 3.8V (min) 32mA UVCCIO = 4.5V	(Standard Version)	Logic Low	0.55V (max) 24mA sink
Digital Outputs Logic High 3.8V (min) 32mA UVCCIO = 4.5V		Power Output	+3.3 VDC via 0.5A polyfuse (resetting)
3 7	TTL w/user VCCIO	1.65V to 5.5V	At DB37M, via polyfuse
(-TTL Option) Logic Low 0.55V (max) 32mA UVCCIO = 4.5V	Digital Outputs	Logic High	3.8V (min) 32mA UVCCIO = 4.5V
	(-TTL Option)	Logic Low	0.55V (max) 32mA UVCCIO = 4.5V

Environmental			
Temperature Operating		0°C to 70°C (order "-T" for -40° to 85°C)	
	Storage	-65° to 150°C	
Humidity	5% to 95%, non-condensing		
Power required	+3.3VDC @ 330mA (typical)		
Physical			
Weight	6.2 grams (+ 22.2g for the cable)		
Size	Length	50.95mm (2.006")	
	Width	30.00mm (1.181")	
I/O connector	On-card	Molex 501190-4017 40-pin latching	
	mating	Molex 501189-4010	
	On cable	Male, D-Sub Miniature, 37-pin	
	mating	Female, D-Sub Miniature, 37-pin	

CHAPTER 9: CERTIFICATIONS

CE & FCC

These devices are designed to meet all applicable EM interference and emission standards. However, as they are intended for use installed on motherboards, and inside the chassis of industrial PCs, important care in the selection of PC and chassis is important to achieve compliance for the computer as a whole.

UL & TUV

Neither DC voltages above 3.3V, nor AC voltages of any kind, are consumed or produced during normal operation of this device. This product is therefore exempt from any related safety standards. Use it with confidence!

ROHS / LEAD-FREE STATEMENT

All models are produced in compliance with RoHS and various other lead-free initiatives.

WARNING

A SINGLE STATIC DISCHARGE CAN DAMAGE YOUR CARD AND CAUSE PREMATURE FAILURE! PLEASE FOLLOW ALL REASONABLE PRECAUTIONS TO PREVENT A STATIC DISCHARGE SUCH AS GROUNDING YOURSELF BY TOUCHING ANY GROUNDED SURFACE PRIOR TO TOUCHING THE CARD.

ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A CARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING

CARDS, INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O CARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

WARRANTY

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations:

GENERAL

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arriving from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to ACCES equipment not approved in writing by ACCES or, if in ACCES opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.

TERMS AND CONDITIONS

If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

COVERAGE

FIRST THREE YEARS: Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment.

FOLLOWING YEARS: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

EQUIPMENT NOT MANUFACTURED BY ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

DISCLAIMER

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PCI EXPRESS MINI CARD STANDARD NOTICE AND EXCEPTION

The mPCI-DIO-24S family of devices are fully compliant with PCI Express Mini Card v1.2.